P24641A Multichannel DSP ASIC for Detector Streaming Readout

Keywords: Detector ROIC, pulse shaper, event builder, multichannel ADC, segmented detectors

Technical Summary

The P24641A is a power efficient 32-channel TID tolerant DSP ASIC for streaming readout of single photon sensitive detectors. Each channel includes a 12-bit 1GS/s ADC for signal digitizing, a DSP block for pulse shaping and, a digital event building back-end with readout through a single 16Gbps JESD204B lane. In addition the main operation mode for detector event processing, the ASIC can operate as a standard 32 channel ADC array with 32 JESD204B standard compliant output data lanes.

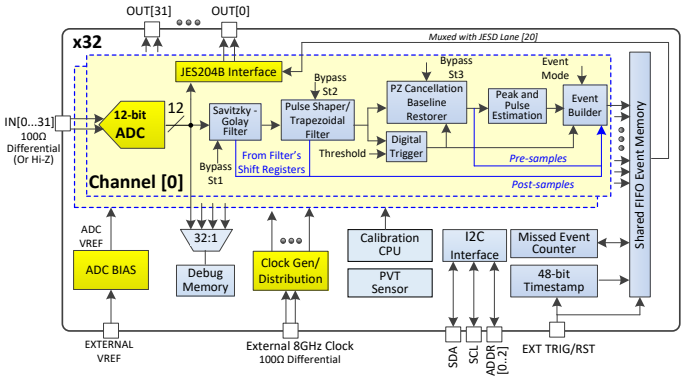

Figure 1. A block diagram of the ASIC.

A block diagram of the ASIC's internal features is shown in Figure 1. The ASIC includes a RISC-V CPU for ADC calibrations and top-level control, including external components through GPIOs. The fabricated die, and a prototype assembled part is shown in Figure 2. Figure 3 shows a characterization board made for initial characterization. An evaluation board will be made for customer evaluation.

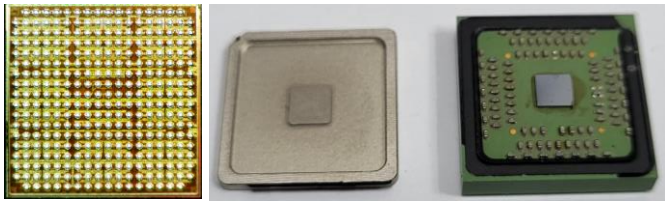

Figure 2. The fabricated chip (left), a lid (middle), assembled part (right).

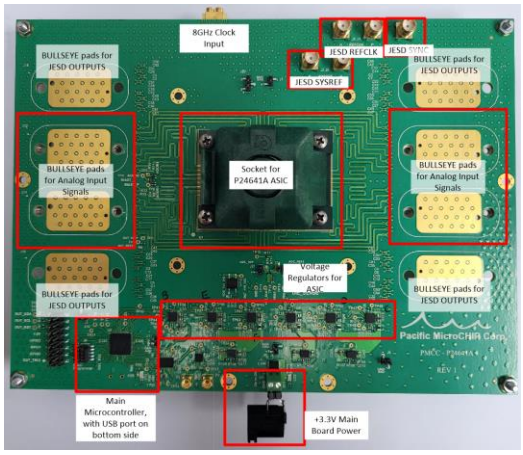

Figure 3. The ASIC testing/evaluation PCB with a socket.

Operational Capabilities

The P24641A is a TID tolerant, low power, compact and low-cost solution for streaming readout of gamma- and X-ray detectors as well as other multichannel single photon sensitive detectors. Specific capabilities include:

- 32 independent 12-bit resolution 1GS/s ADCs.
- Approximately 7bits ENOB across first Nyquist zone.
- >65dB SFDR
- >700MHz -3dB Bandwidth
- 16Gbps JESD204B compliant output for each ADC.
- Each ADC has A DSP block for pulse shaping and baseline restoration.
- Event builder uses a single JESD204B lane for readout, streaming out up to 100M events per second.
- Event builder has two modes of operation: pulse parameters or pulse samples.
- Pulse parameter mode records the time of pulse, time over threshold, peak value, time to peak
- Pulse sample mode records time of pulse, and 16 samples with user defined number pre- and post-samples.
- Power consumption of about 119mW/ch with JESD204B interface
- On-chip RISC-V CPU can be used for ADC calibration and top-level control using GPIOs.
- I2C interface for accessing ASIC's internal control/status registers.
- On-chip PVT sensor can be used to measure die temperature or external DC voltages.
- Tested through -45°C ~ 120°C die temperature.

Potential Applications

- Readout of SiPMs and PMTs used in calorimeters
- Segmented gamma- and X-ray spectroscopy systems
- Test and measurement instrumentation
- Multichannel data acquisition devices
- Synthetic aperture spectrometers, radars and lidars
- Medical and industrial CT scanners
- Pulsed Radars

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