A Multichannel DSP ASIC for Streaming Readout

Keywords: Detector ROIC, pulse shaper, pulse builder, multichannel ADC, sensor arrays

Technical Summary

Pacific Microchip Corp. is developing a power efficient 32-channel TID tolerant DSP ASIC for streaming redout of single photon sensitive detectors. The chip will include 12-bit 1GS/s ADC for signal digitizing, a DSP block for pulse shaping and, a digital event building back-end. In addition to its main operation mode for detector event processing, the ASIC will operate as a regular ADC array with a JESD204B standard compliant output data interface.

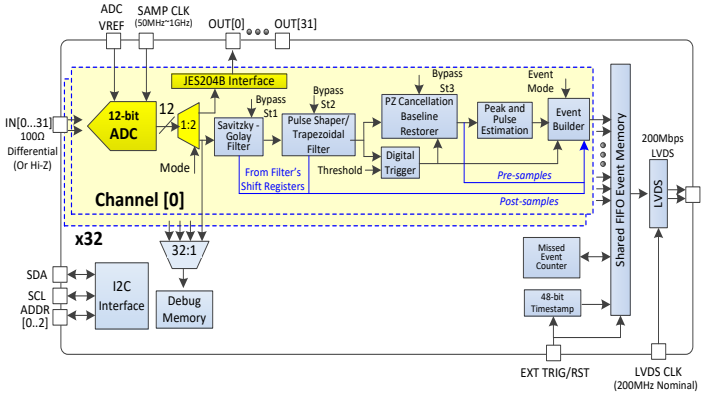


Figure 1. A block diagram of the ASIC.

The ASIC will support streaming data readout of single photon sensitive detector instruments. The standalone ADC operation mode with data output through the JESD204B standard interface is expected to increase the commercialization potential. The ADC is built following the hybrid SAR/Pipeline architecture. ADC calibration is performed using an on-chip CPU.

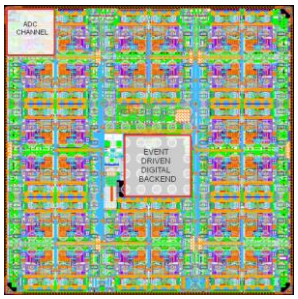


Figure 2. Expected view of the chip layout.

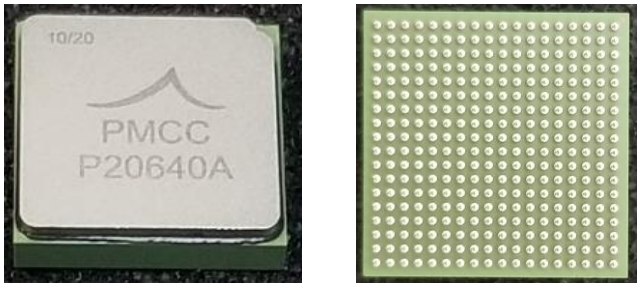


Figure 3. Expected view of the ASIC in a BGA package (left) and the ball array (right).

Operational Capabilities

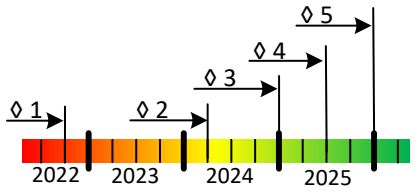
Our product will provide a TID tolerant, low power, compact and low-cost solution for streaming readout of gamma- and X-ray detectors as well as other multichannel single photon sensitive detectors. Specific capabilities include:

- A DSP block for:
  - Digital filters for pulse shaping;
  - Baseline restoration;
- Event builder function:
  - Automatic triggering, time-stamping;
  - Digital detection of pulse time-to-peak, duration and amplitude;
  - Event building, >30k events per channel.
  - Waveform capture (pre- and post-event)
  - LVDS Interface for data output
- Silicon proven ADC IP:
  - 32 channels, 12-bit, up to 10-bit ENOB at 1GS/s;
  - JESD204B standard compliant output data interface;
- Independent operation of the 32-channel ADC.
- Extended temperature range -40…125°C.
- Power consumption of 42.5mW per channel.

Development Objectives & Milestones

Through the DoE Phase I project, Pacific Microchip Corp. will demonstrate the feasibility of the ASIC implementation. In Phase II (if granted), the chip will be designed, produced, packaged and tested. The project milestones include:

◊ 1. ASIC feasibility is proven based on simulations
◊ 2. ASIC chip is designed and taped out
◊ 3. The chip is fabricated and tested
◊ 4. Final chip is designed and taped out
◊ 5. Final chip is fabricated, tested, and sales started



Applications

- Readout of SiPMs used in calorimeters at the EIC
- Multichannel gamma-ray spectroscopy systems (DoE)
- X-ray detectors (DoE)
- Synthetic aperture spectrometer instruments (NASA)
- Test and measurement instrumentation
- Multichannel data acquisition devices
- Synthetic aperture radars and lidars
- Medical and industrial CT scanners

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