Polarimetric Spectrometer ASIC

Keywords: Polarimetric spectrometer ASIC, Earth observation, polyphase filter, FFT, ADC

Technical Summary

The P23801A polarimetric spectrometer ASIC processes two 10GHz bandwidth (H/V) input signals from RF front ends. Signal spectrum is channelized into 4,096 frequency bins, the frequency-domain results of each channel are converted to the power and relative phase, and then accumulated. The analog front ends include VGAs and 6-bit ADCs. The digital back ends include data alignment blocks, PFB based FFT cores, accumulators and cross-channel analysis functions. The chip also includes an output data interface, a PLL based clock synthesizer and an SPI interface for the ASIC's programming and data interchange at low speed (Fig.1). The chip is offered in a BGA package (Fig.2). The ASIC (P23801A) will be offered as a component and as a bord level solution (Fig.3). Fig. 4 shows measured ASIC performance results.

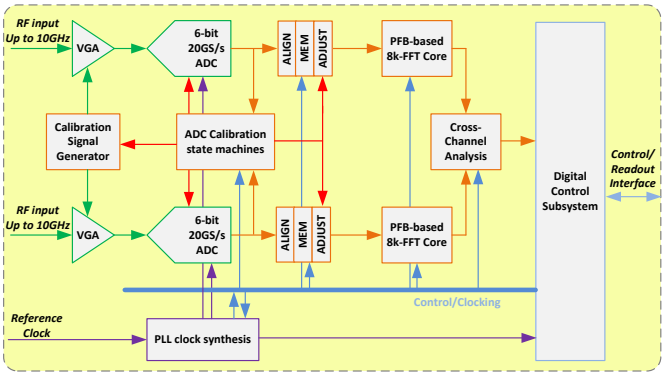


Figure 1. A block diagram of the ASIC.

Figure 2. The view of the chip and expected view of the BGA package.

TBD

Figure 3. An evaluation PCB.

TBD

Figure 4. Demonstration of ASIC functionality.

Operational Capabilities

The ASIC includes 2 channels that digitize the RF signal and split spectrum into 4,096 frequency bins, thus, achieving 2.44MHz spectral resolution. Specific capabilities/features:

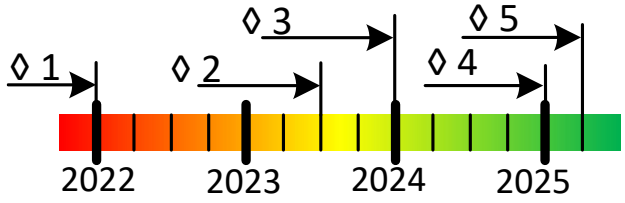
- Input signal bandwidth up to 10GHz
- Sampling rate up to 20GS/s
- Input signal FSR programmable from 100mV to 400mV pp differential
- Digitizer ENOB > 4-bit to 10GHz
- Power consumption < 4W (full functionality)
- 4,096 frequency bins within 0 to 10GHz
- Output data is power level and relative phase
- Accumulation time programmable from 1us to 1s
- An integrated 20GHz PLL, selectable Fref
- An SPI interface for control, diagnostics and readout
- Temperature range -40°C to 125°C
- 15 x 15 BGA package (12.8mm x 12.8 mm)
- Fabrication technology 28nm CMOS

Development Objectives & Milestones

P23801A polarimetric spectrometer ASIC implementation feasibility is being explored. Further, the ASIC chip will be designed, fabricated, packaged, and tested. The part and an evaluation PCB will be available for purchasing. In case further improvements are required, the Rev 2 ASIC will be designed, fabricated, tested and provided to the customers.

The project includes the following milestones:

◊ 1. Feasibility is proven based on simulations.
◊ 2. Rev 1 prototype ASIC chip is designed and taped out.
◊ 3. Rev 1 ASIC is fabricated/tested, being sampled.
◊ 4. Rev 2 ASIC is fabricated (if funding is available).
◊ 5. Rev 2 ASIC is tested (if funding is available), sales started.



Current TRL: 3, Estimated final TRL: 6

Applications

- Remote sensing instruments
- Radio astronomy
- Planetary exploration missions
- Synthetic aperture radiometers
- Spectrum analyzers

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