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Technical Summary

The P24803A frequency channelizer ASIC processes incoming I/Q signal up to 1GHz bandwidth (I/Q) into 2048 frequencyselectable bins for further phase/power measurement in each (Fig.1). The signal digitized in two 12-bit 1GS/s ADCs is passed through a block including data alignment, ADC calibration, and debug memory. The aligned data is fed to 2048 DFT cells which compute the user-configurable frequency bins, and very-finely adjustable frequency with <1KHz precision. The data representing the real/imaginary components within the selected frequency bins is read out through the RGMII interface. The chip also includes a PLL based frequency synthesizer and an I²C interface for the ASIC's programming/control and data interchange at low speed. The chip (Fig.2) is offered in a BGA package and as an IP block for integration into SoCs. The P24803A ASIC is also offered on an evaluation board (Fig.3). Fig. 4 shows measured ASIC performance results.



Figure 1. A block diagram of the ASIC.



Figure 2. The ASIC chip and the BGA package.



Figure 4. An example - ASIC readout, Fin = 1GHz (I/Q).

Operational Capabilities

The ASIC digitizes the I/Q signal and computes 2048 frequencyselectable bins. The resulting complex values can be read out through the high-speed interface.

- Input signal bandwidth up to 1GHz (I/Q)
- Sampling rate up to 1GS/s (each channel)
- Input signal FSR programmable from 250mV to 550mV pp differential
- Digitizer ENOB > 10-bit
- Power consumption < 3.5W (full functionality)
- 2048 frequency-selectable bins over 1GHz bandwidth
- Frequency resolution 953.67 Hz
- Sampling time selectable between 0.5ms or 1ms
- An integrated PLL with selectable Fref
- An I²C interface for control, diagnostics and readout
- An RGMII interface for control and readout
- Temperature range -40°C to 110°C
- 15 x 15 BGA package (12.8mm x 12.8 mm)
- Fabrication technology 28nm CMOS

Development Objectives & Milestones

P24803A frequency channelizer ASIC will be designed, fabricated, packaged and tested. The part and an eval PCB will be available for purchasing. In case if any further improvements are required, the modified ASIC will be designed, fabricated, tested and made available to the customers.

The project includes the following milestones:

- ◊ 1. Project kick-off
- ◊ 2. Feasibility is proven based on simulations
- ♦ 3. Prototype ASIC chip is designed and taped out
- ♦ 4. ASIC is fabricated/tested, being sampled
- ◊ 5. Revised ASIC is fabricated/tested, sales started



Current TRL: 2, Estimated final TRL: 6

Applications

- Remote sensing instruments
- Hyperspectral astronomy
- Planet and Sun exploration missions
- Synthetic aperture radiometers
- Spectrum analyzers