P24802A 28GHz Spectrometer ASIC

Keywords: Spectrometer ASIC, spectrum analyzer, radio astronomy, FFT, ADC

Technical Summary

The P24802A spectrometer ASIC processes up to 28GHz bandwidth input signals provided by microwave front ends. The ASIC (Fig.1) includes an AFE, an 8-bit 56GS/s ADC, an FFT based on polyphase filtering and an accumulator capable of accumulating up to 0.5 seconds of frequency-domain data. The chip also includes an output data interface, a PLL based frequency synthesizer and a I^2C interface for the ASIC's programming/control and data interchange at low speed. The chip (Fig.2) is offered in a BGA package and as an IP block for integration into SoCs. The P24802A ASIC is also offered on an evaluation board (Fig.3). Fig. 4 shows measured ASIC performance results.

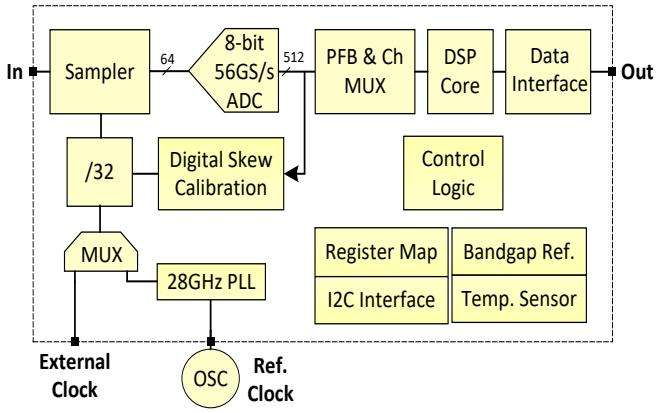


Figure 1. A block diagram of the ASIC.

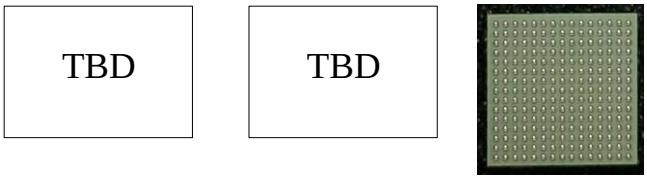


Figure 2. The ASIC chip and the BGA package.

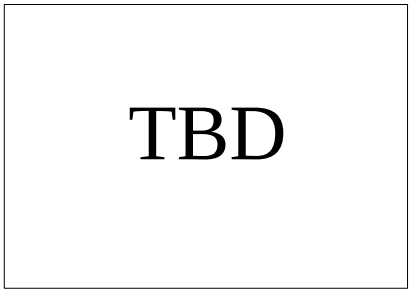


Figure 3. ASIC evaluation board.

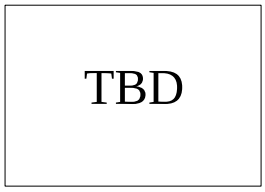


Figure 4. An Example - ASIC readout with Fin = 28GHz.

Operational Capabilities

The ASIC digitizes the RF signal and in the first stage splits the spectrum into 32 sub-bands. Then each sub-band is divided into 1024 frequency bins. The power is computed for each bin and the result is accumulated.

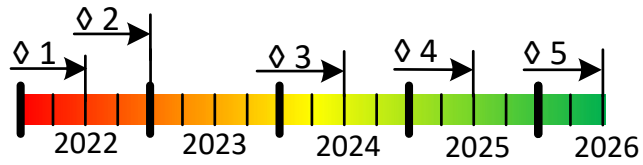
- Input signal bandwidth up to 28GHz
- Sampling rate up to 56GS/s
- Input signal FSR programmable from 250mV to 550mV pp differential
- Digitizer ENOB > 6-bit to 28GHz
- Power consumption < 3W (full functionality)
- Up to 2048 frequency bins within 1.75GHz of input frequency
- Accumulation time programmable from 1.1us to 0.5s
- An integrated 28GHz PLL with selectable Fref
- An I^2C interface for control, diagnostics and readout
- Temperature range -40°C to 110°C
- 15 x 15 BGA package (12.8mm x 12.8 mm)
- Fabrication technology 28nm CMOS

Development Objectives & Milestones

P24802A spectrometer ASIC will be designed, fabricated, packaged and tested. The part and an eval PCB will be available for purchasing. In case if any further improvements are required, the modified ASIC will be designed, fabricated, tested and made available to the customers.

The project includes the following milestones:

◊ 1. Project kick-off
◊ 2. Feasibility is proven based on simulations
◊ 3. Prototype ASIC chip is designed and taped out
◊ 4. ASIC is fabricated/tested, being sampled
◊ 5. Revised ASIC is fabricated/tested, sales started



Current TRL: 2, Estimated final TRL: 6

Applications

- Remote sensing instruments
- Radio astronomy
- Planet and Sun exploration missions
- Synthetic aperture radiometers
- Spectrum analyzers

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