A 32 Channel ASIC for X- and Gamma-Ray Energy and Timing Measurement

Keywords: Event building, Streaming readout, X-ray detector readout, Gamma-ray detector readout

Technical Summary

Pacific Microchip Corp. has developed a power efficient 32-channel ASIC for X- and gamma-ray energy and timing measurement with a digital event building back-end.

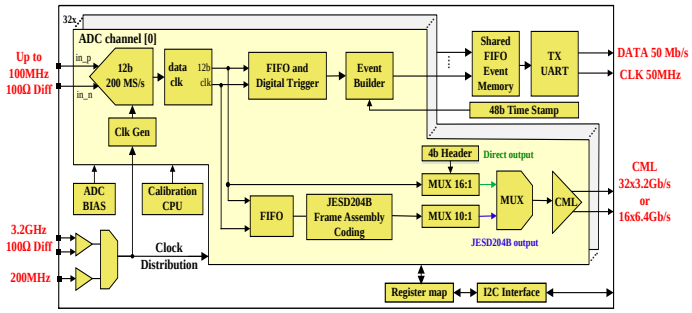


Figure 1. A block diagram of the ASIC.

Figure 2. A Chip photo (left), BGA package (center) and the ball array (right).

The ASIC is targeted to support applications in single photon sensitive detector instruments for event related energy and timing measurement. To increase the commercialization potential, the ADC array built into ASIC includes a JESD204B standard interface for operating the ASIC as an ADC array.

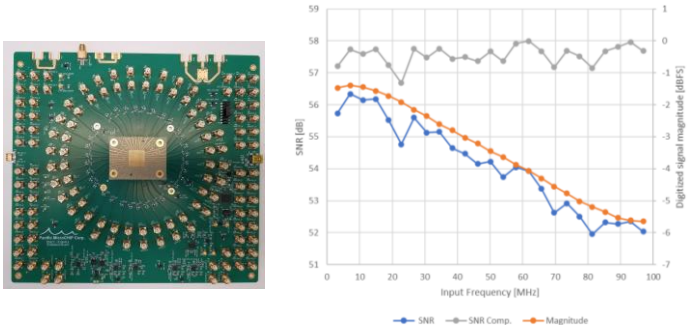


Figure 3. Evaluation PCB and measured ADC parameters.

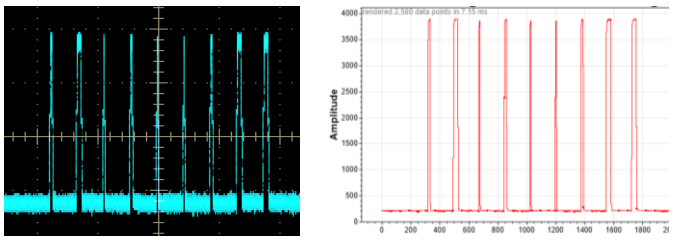


Figure 4. Pulses supplied to the ASIC channel (left). Pulses reconstructed from event builder data (right).

Targeted Operational Capabilities

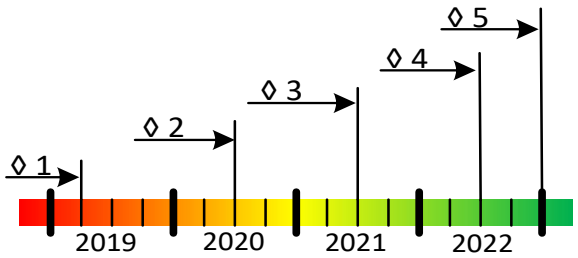
The ASIC offers low power consumption (4.5mW/ch) combined with complex functionality required for signal digitizing and extracting of event related data (time of arrival, threshold, time of peak, peak value, time over threshold, etc.). This data is assembled into packets and shipped out through an UART interface. Specific parameters/capabilities:

- 32 independently operated channels
- Programmable sampling rate of 200/100/50 MS/s
- 1Vpp differential input swing
- Digitizing ENOB > 10-bit
- Input signal bandwidth > 0.2GHz
- Integrated 32ch event-building digital back-end
- Optional direct ADC output through JESD204B interface
- Event data packet output through UART interface
- Power consumption < 4.5mW/channel (JESD204B is off)
- Total power with ADC data interface <880mW.
- I2C interface for ASIC control
- Chip layout footprint 7.8mm^2
- 15mm x 15mm 361 ball BGA package

Development Objectives & Milestones

The Phase I project demonstrated the feasibility of the ASIC. Currently, the Project is in its Phase II – the ASIC 1st prototype was designed, fabricated and tested. The project milestones include:

◊ 1. Feasibility is proven based on simulations (Ph. I)
◊ 2. Prototype ADC chip is designed and taped out (Ph. II)
◊ 3. Prototype chip is fabricated and tested (Ph. II)
◊ 4. Final chip is designed and taped out (Ph. IIA/B)
◊ 5. Final chip is fabricated, tested, and sales start (Ph. IIA/B)



Applications

- Multichannel gamma-ray spectroscopy systems (DoE)
- X-ray detectors (DoE)
- CT systems, luggage, and cargo scanners
- Synthetic aperture spectrometer instruments (NASA)
- Test and measurement instrumentation
- Multichannel data acquisition devices
- Synthetic aperture radars and lidars

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