Correlation Radiometer ASIC

Keywords: Correlation radiometer, radiometer ASIC, Earth observation, polyphase filter, ADC

Technical Summary

This project aims to develop an ASIC for the NASA's microwave correlation radiometers required for space and airborne Earth observation missions. The ASIC is expected to operate with the microwave front ends down-converting the RF to up to 10GHz IF quadrature signals (Fig.1). The ASIC includes VGAs, digitizers, deserializers, bandpass filters, cross-correlators, totalizers, an output data interface and an I2C interface for the ASIC's programming (Fig.2). Bandpass filters on the ASIC split up the digitized quadrature IF input signals into bands (up to 31). Further, the signals are cross-correlated within each band, and the resultant data is shipped out in a convenient format. Instead of analog signal processing performing a strictly defined function, the ASIC employs a digital signal processing which can be reprogrammed to adopt specific parameters of the filter block. The ASIC will be offered as a separate component and as an IP block for integration into SoCs.

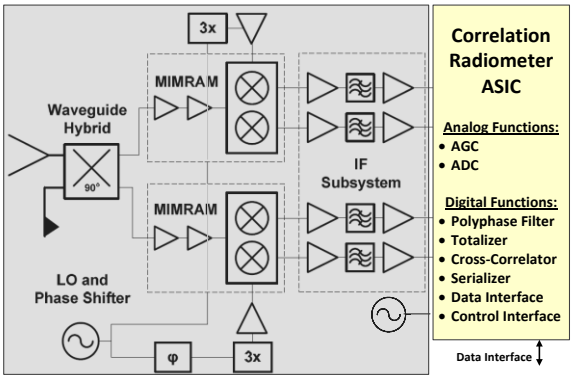


Figure 1. The ASIC in the correlation radiometer system.

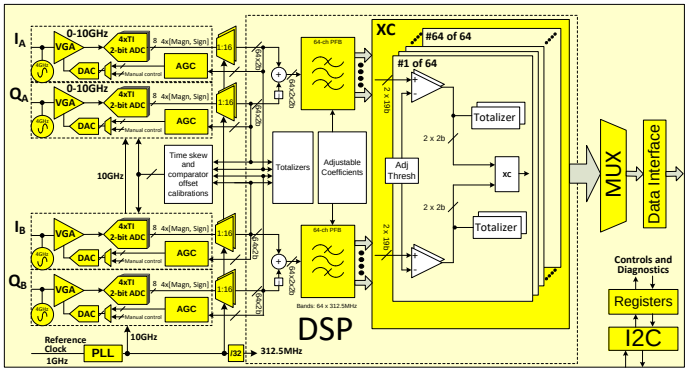


Figure 2. A block diagram of the ASIC.

The ASIC will be supplied in a LTCC BGA chip package (Fig. 3). An evaluation board will be supplied to selected customers.

Figure 3. The ASIC in a BGA package.

Operational Capabilities

The ASIC simplifies the radiometer system by reducing its weight, power consumption, cost and complexity. Specific capabilities/features include:

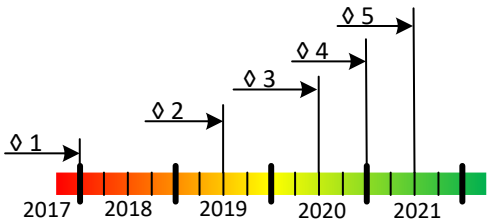
- Input signal bandwidth 20GHz (I/Q, total)
- Input signal level -25dBm to -15dBm
- Sampling rate up to 20GS/s
- Digitizer ENOB > 1.5-bit
- ASIC power consumption < 1.6W
- Polyphase filter bands up to 31
- Cross-correlation of signals as: II, QQ, IQ and QI separately within each band
- 4x16 totalizers counting the number of occurrences of each 2-bit input signal values (-3, -1, 1, 3)
- Accumulation time from 0.1ms to 100ms
- An integrated 10GHz PLL
- An I2C interface for control, diagnostics and readout
- 15 x 15 BGA package (12.8mm x 12.8 mm)
- Fabrication technology 28nm CMOS

Development Objectives & Milestones

Pacific Microchip Corp. has demonstrated the feasibility, designed, and is currently fabricating the chip. Further, the chip will be packaged, tested, and the part will be sampled to selected customers. Based on the testing results, the chip will be redesigned (subject to availability of funds), retested, and its production will be started.

The project includes the following milestones:

◊ 1. Feasibility is proven based on simulations
◊ 2. Prototype ASIC chip is designed and taped out
◊ 3. Prototype chip is fabricated/tested and being sampled
◊ 4. Final/customized chip is designed and taped out
◊ 5. Final chip is fabricated, tested, and sales are started



Current TRL: 3, Estimated final TRL: 5

Applications

- Remote sensing instruments
- Radio astronomy
- Planet and Sun exploration missions
- Distributed spacecraft missions
- Communication and navigation satellites
- Synthetic aperture radars and radiometers

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