ASIC Based Correlation Radiometer

Keywords: Correlation radiometer, radiometer ASIC, Earth observation, polyphase filter, ADC

Technical Summary

The project relies on previously developed correlation radiometer solution which included an analog processing part on an ASIC, while the DSP part was implemented on an FPGA. Previous solution was able to operate at 0.004% duty cycle. This project aims to develop an ASIC including entire (analog and digital) processing for microwave correlation radiometers operating at 100% duty cycle (Fig.1). These instruments are required for space and airborne Earth observation missions. The DSP block the ASIC employs can be reprogrammed to adopt specific parameters of the filter block. Bandpass filters on the ASIC split up the digitized quadrature IF input signals into bands (up to 31). Further, the signals are cross-correlated within each band, and the resultant data is shipped out in a convenient format. We will offer to our customers the ASIC and a board level solution (Fig. 2) based on the developed ASIC.

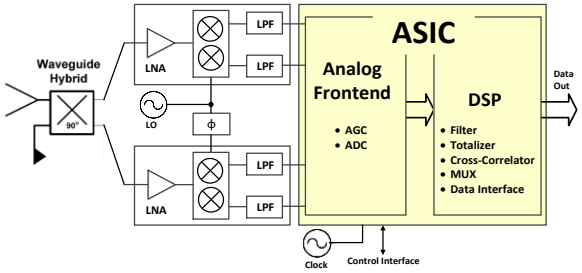


Figure 1. The ASIC in the correlation radiometer system.

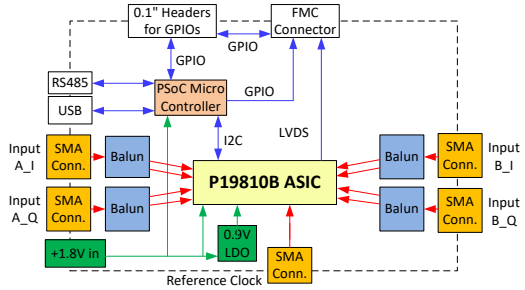


Figure 2. A block diagram of the ASIC based radiometer solution.

The chip is assembled in an LTCC BGA chip package (Fig. 3). An evaluation board (Fig. 4) will be supplied to selected customers.

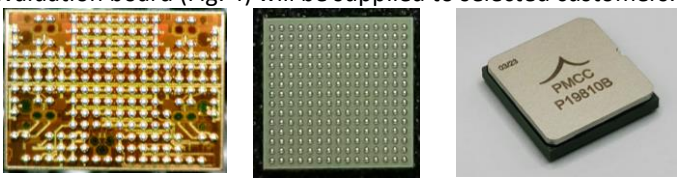


Figure 3. Fabricated chip (left), BGA (center), and expected packaged part view (right).

Operational Capabilities (Expected)

The ASIC facilitates the radiometer system to reduce its weight, power consumption, cost and complexity by applying DSP instead on analog signal processing. Specific capabilities include:

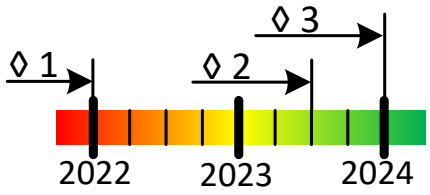
- Input signal bandwidth 20GHz (I/Q, total)
- Input signal level -30dBm to 0dBm
- Sampling rate up to 20GS/s
- Four 2-bit ADCs sampling at up to 20GS/s
- Digitizer ENOB > 1.5-bit
- 64 sub-band PFB with programmable coefficients
- ASIC power consumption < 1.6W
- 64 sub-band PFB with programmable coefficients
- Cross-correlation of signals as: II, QQ, IQ and QI separately within each band
- 4x16 totalizers counting the number of occurrences of each 2-bit input signal values (-3, -1, 1, 3)
- Accumulation time from 0.1ms to 100ms
- An integrated 10GHz PLL
- An I2C interface for control, diagnostics and readout

Development Objectives & Milestones

Previously Pacific Microchip Corp. has demonstrated the feasibility, designed, fabricated, packaged, and tested the Gen 1 prototype ASIC. Further, the feasibility of the Gen 2 ASIC was demonstrated. Currently the Gen 2 ASIC is being modified to address identified issues. Once fabricated, the ASIC will be tested, and provided for customers.

The project includes the following milestones:

◊ 1. Feasibility of Gen 2 ASIC is proven based on simulations
◊ 2. Prototype Gen 2 ASIC is designed and taped out
◊ 3. Prototype Gen 2 chip is fabricated/tested



Current TRL: 3, Estimated final TRL: 6

Applications

- Remote sensing instruments
- Radio astronomy
- Planet and Sun exploration missions
- Distributed spacecraft missions
- Communication and navigation satellites
- Synthetic aperture radars and radiometers

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