JaTc and TOWER conference

Pacific MicroCHIP Corp.

Thermal Gradient and IR Drop Aware Design Flow for Analog-Intensive ASICs

Pacific MicroCHIP Corp.

AIMS-CAT November, 2009

OUTLINE

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- Thermal Gradient Impact Simulation
  - Methodology
  - Results
- Accurate IR Drop Simulation
  - Methodology
  - Results
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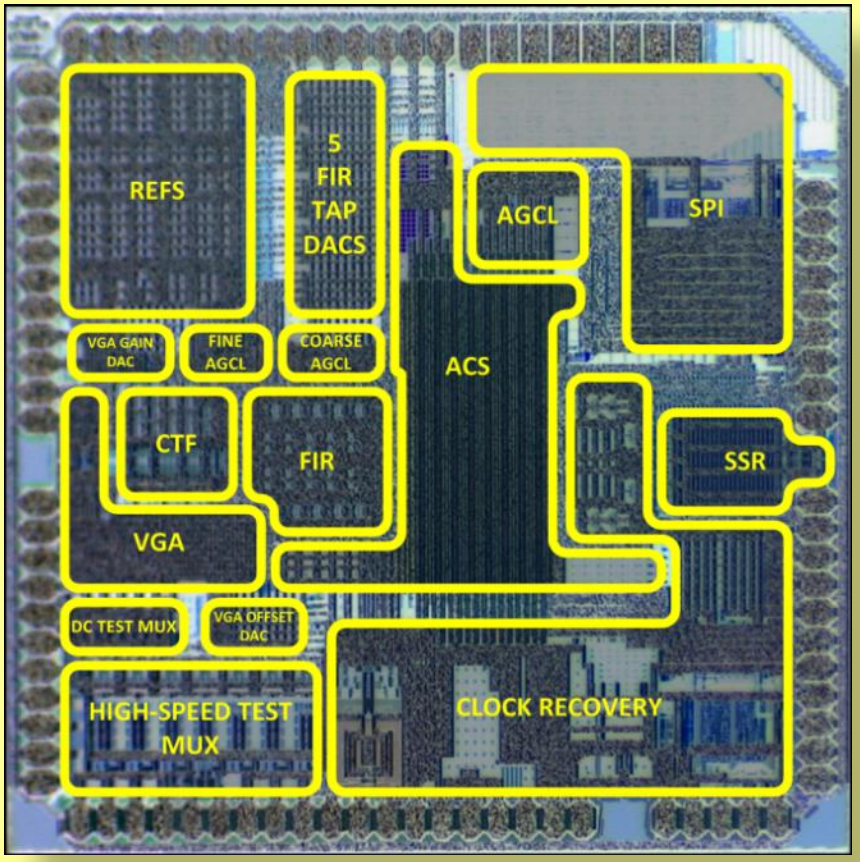
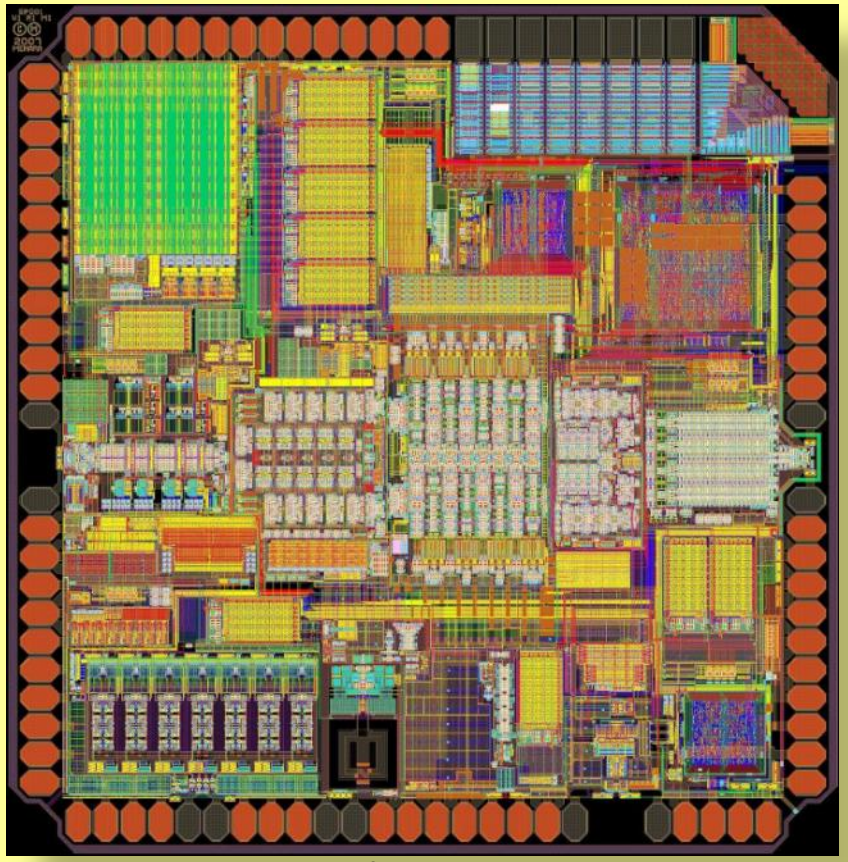
THERMAL GRADIENT IMPACT SIMULATION METHODOLOGY

Motivation

What : PRML based EDC fiber-optic receiver ASIC built on Jazz SiGe120 process.
Why : Analog accuracy of 10mV at 10Gbps comes with price: 4.5W on a 2.5x2.5mm die.
Goal 1: Simulate die thermal gradient and evaluate its impact on IC performance.
Goal 2: Simulate grid IR drop and verify the impact on IC performance and reliability.



ASIC photo with outlined top level blocks



ASIC layout view

THERMAL GRADIENT IMPACT SIMULATION METHODOLOGY

Step #1. Data entering

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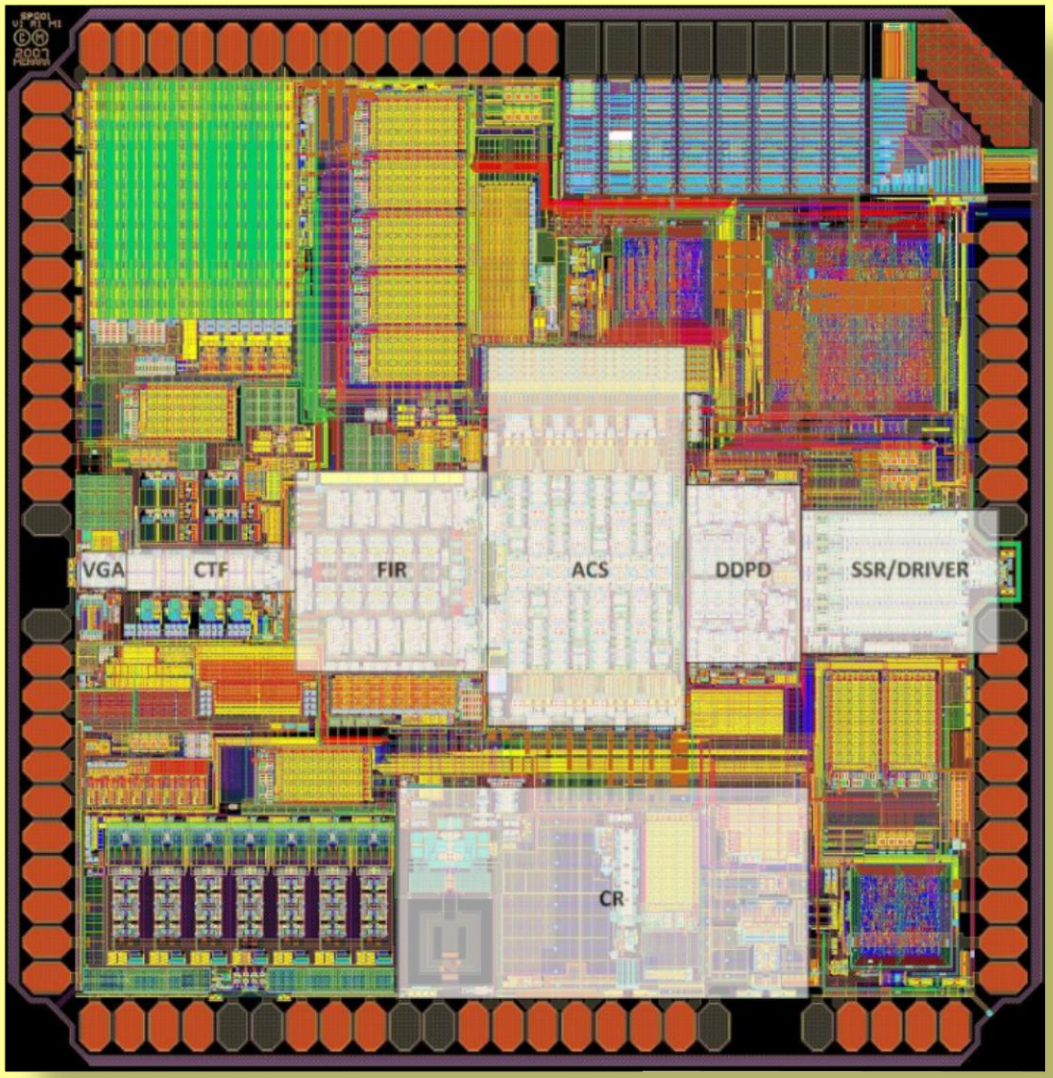
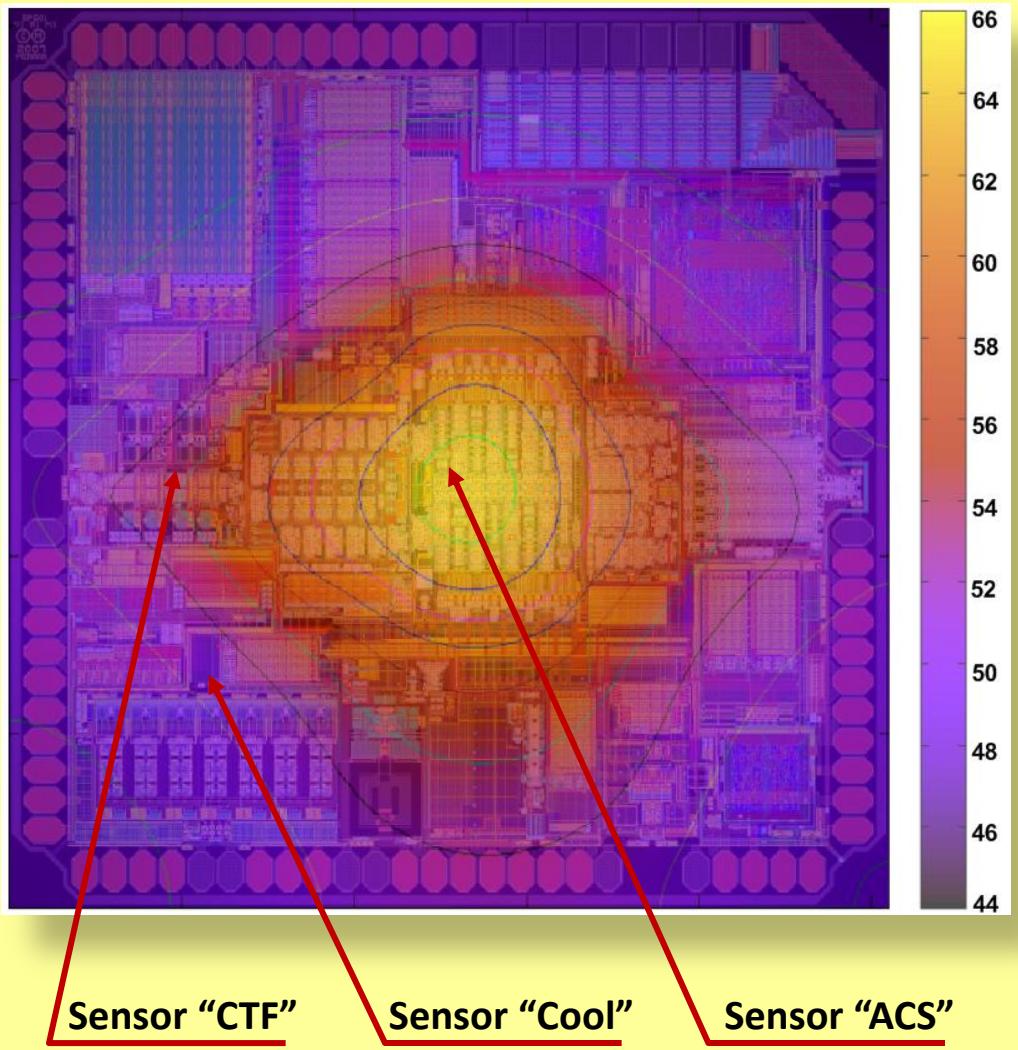


1. Identify main blocks - heat sources
2. Enter their coordinates and corresponding power levels to thermal simulation software
3. Enter package and heatsink geometry and thermal data (optional)

Block geometry and power dissipation

Block	Width	Height	X0	Y0	P [W]
CR	710	403	1170	199	0.50
SSR	457	326	1853	952	0.32
DDPD	270	403	1583	930	0.30
ACS	464	861	1119	786	2.32
FIR	445	458	674	908	0.92
CTF	394	98	280	1091	0.22
VGA	110	83	170	1100	0.06

THERMAL GRADIENT IMPACT SIMULATION METHODOLOGY
Step #2. Thermal gradient simulation



Thermal gradient overlaid on the ASIC layout shows:

- 22°C gradient hot-spot to chip corner
- 8°C gradient across FIR and ACS blocks.

Simulation results are verified based on three on-chip temperature sensors.

Measured data closely matches simulated:

Sensor “ACS” – Sensor “CTF”: 21°C
Sensor “CTF” – Sensor “Cool”: 2°C

THERMAL GRADIENT IMPACT SIMULATION METHODOLOGY

Step #3. Thermal gradient mapping

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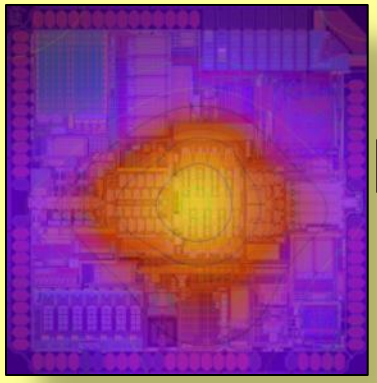
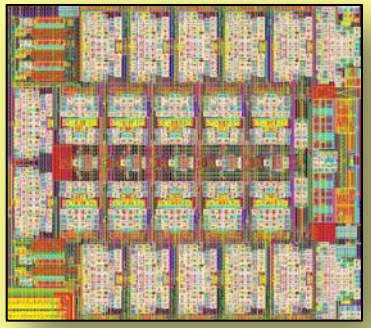
An In-house developed Skill based tool maps of thermal gradient on the post-layout netlist.

Input data:

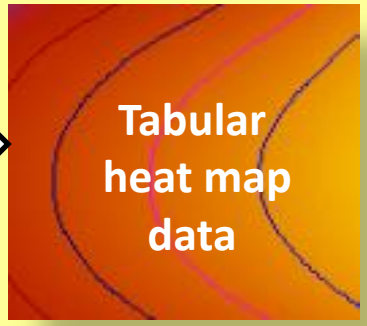
1) RCX extracted views (Calibre or Assura) of LVS clean layout blocks
2) blocks positions on the die
3) Thermal gradient information (simulated, measurement or estimated)

Output data: netlist with temperature rise values added to the active and passive components.





LVS clean layout



Calibre
or
Assura
Extracted view

Thermal gradient mapping tool

Extracted view with applied Δt to components' "temprise" property

The mapping tool assigns the Δt to extracted devices "temprise" property used in the Spectre model:

```
temprise=heatmap[I:J]
```

where:

`heatmap` – 2D array from thermal simulation,
`I=int(X/grid_step)` –map column,
`J=int(Y/grid_step)` –map row.

Coordinates X and Y values are taken from devices "xy" property assigned by extraction tool.

THERMAL GRADIENT IMPACT SIMULATION METHODOLOGY

Step #4. Electrical simulation – verification of gradient impact

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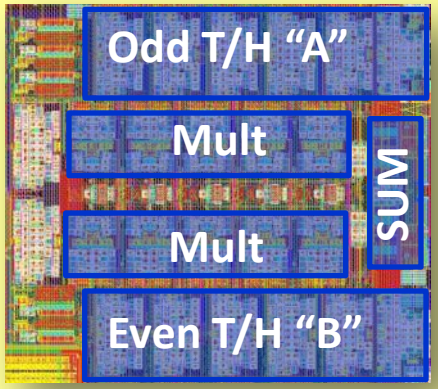
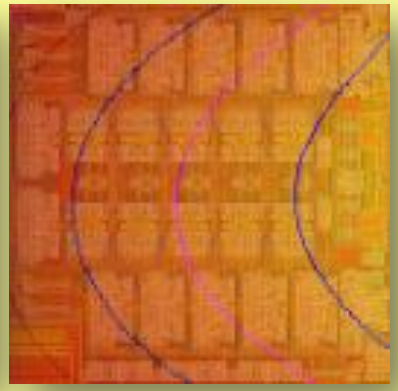




PRML ASIC FIR:

- 11.5Gbps 5-TAP Filter
- Interleaved architecture
- Thermal gradient across multipliers is ~5°C

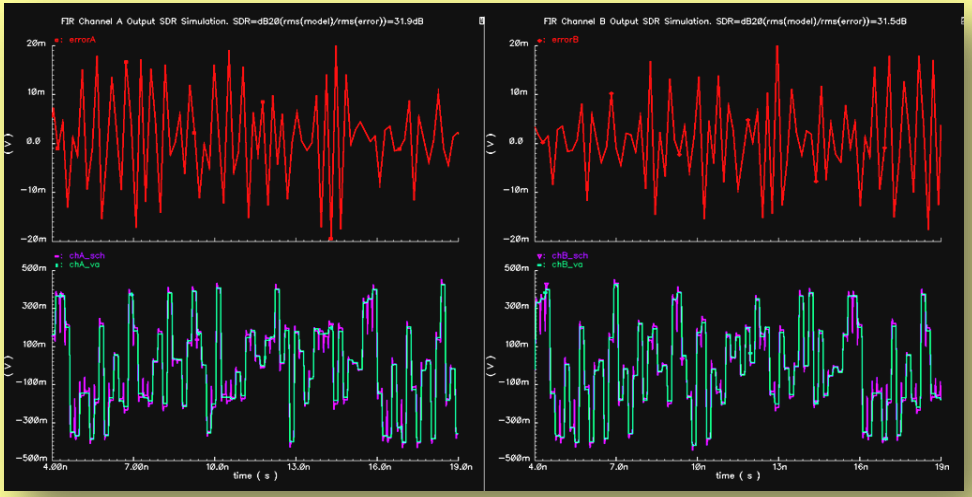
SIMULATION RESULTS:

no thermal gradient (upper graph),

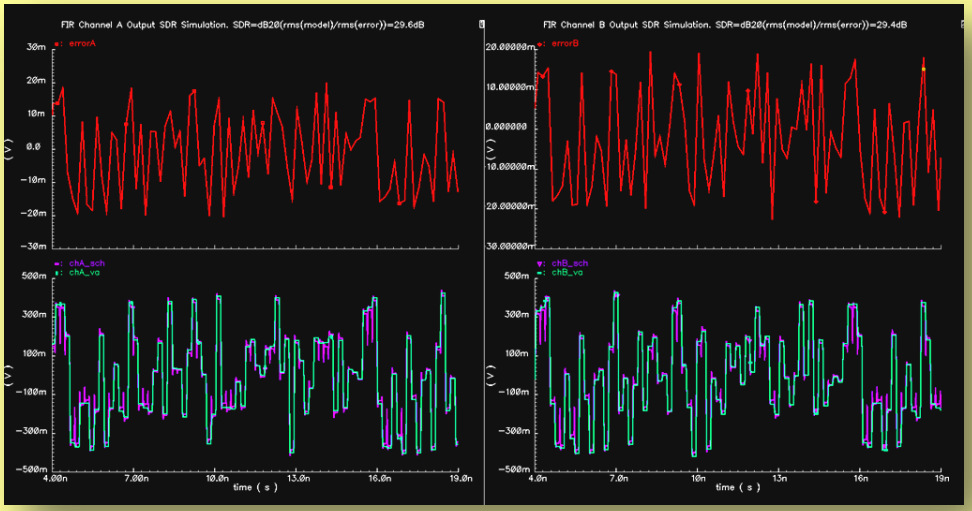
with thermal gradient (lower graph).

- Signal Distortion Ratio is derived by comparing schematic FIR output to the Verilog-A FIR model.
- Same test bench and simulator settings were used.
- Thermal gradient impact degrades SDR by ~2dB.
- Layout is optimized by placing odd and even channels symmetrically with respect to thermal gradient.
- SDR degradation is fixed by adjusting FIR taps.

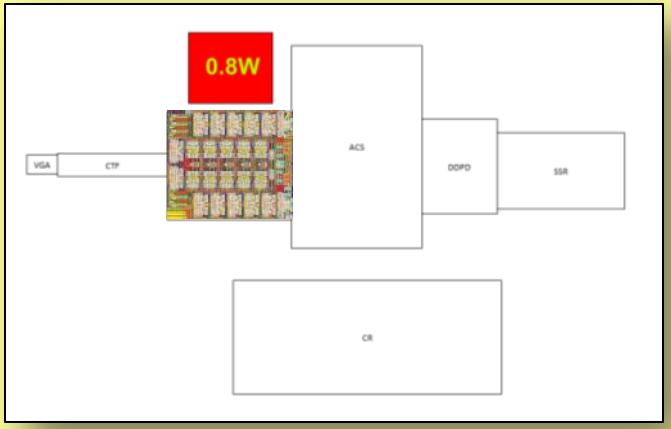
no thermal gradient: SDR_A=31.9dB, SDR_B=31.5dB



with thermal gradient: SDR_A=29.6dB, SDR_B=29.4dB

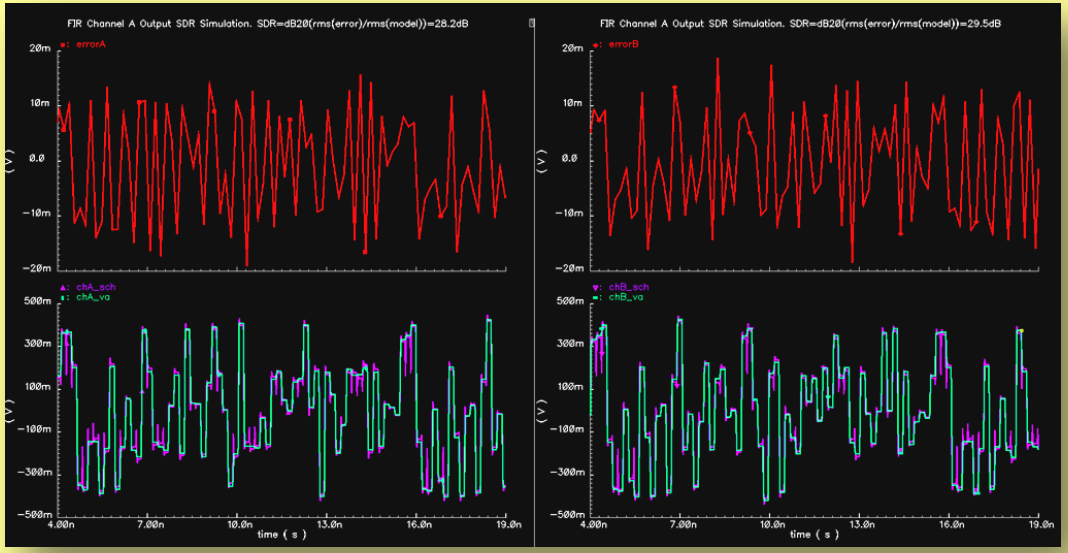


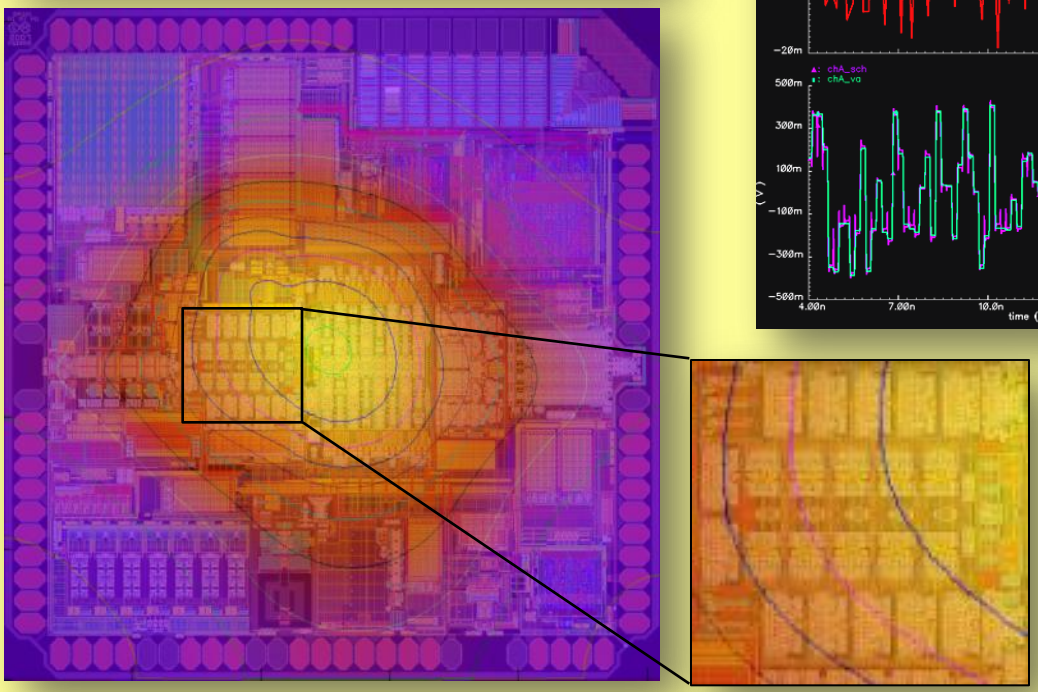
THERMAL GRADIENT IMPACT SIMULATION METHODOLOGY
Thermal gradient aware floorplanning demonstration



-- Additional 300um X 300um block consuming 0.8W is introduced near the FIR on the ASIC floorplan. Resulting thermal gradient was annotated to FIR netlist for SDR simulation.

Simulation results: SDR_A=28.2dB, SDR_B=29.5dB





-- Thermal gradient has a different impact on odd and even FIR interleaves' multipliers and T/H, causing ~1.6dB difference in SDR for FIR channel A and B. Such difference can be partially mitigated by FIR coefficients adjustment.

THERMAL GRADIENT IMPACT SIMULATION METHODOLOGY
Summary

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- We presented thermal gradient impact simulation methodology.
- Methodology is pluggable into analog IC design flow making it thermally aware.
- Demonstrated thermal gradient impact on signal distortion ratio of 11.1Gbps FIR within PRML fiber optics receiver ASIC. Shown how FIR layout and ASIC floorplan optimization mitigated impact of thermal gradient.
- Demonstrated thermal aware floorplaning helping to avoid potential performance issues at the early ASIC design stage.

ACCURATE IR DROP SIMULATION METHODOLOGY

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Main idea is to plot an IR drop map using Spectre DC simulations of Calibre/Assura extracted view of power grid. Accurate simulation requires actual current sources to be taken into account. Can be done 2 ways:

1) **Use entire ASIC R-only extracted view to run DC simulation**
   - ☺ Simple, brute-force solution
   - ☹ Simulator convergence issues
   - ☹ Time consuming
   - ☹ Separate test bench is needed

2) **Use extracted views of main current consuming blocks with embedded ASIC power grid to run multiple DC simulations and combine results**
   - ☹ Requires initial data preparation
   - ☺ Guaranteed to be simulate-able if you can simulate block itself
   - ☺ Less time consuming. Simulations can be run in parallel
   - ☺ Blocks simulation benches can be re-used

ACCURATE IR DROP SIMULATION METHODOLOGY
Step #1: Initial Data Preparation

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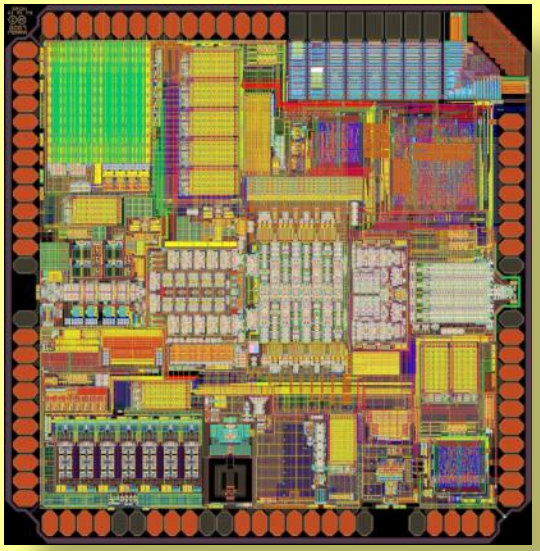
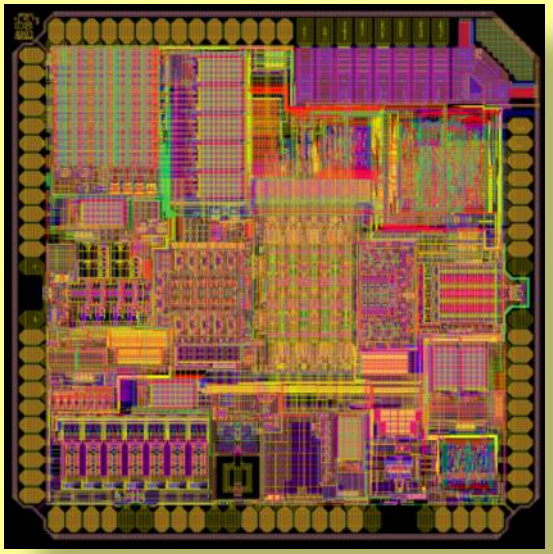
Entire ASIC metallization is extracted into separate layout cell which will be instantiated into each of the blocks for RCX extraction and DC simulation.

Ground plane of PRML based EDC fiber-optic receiver ASIC is used for demonstration.

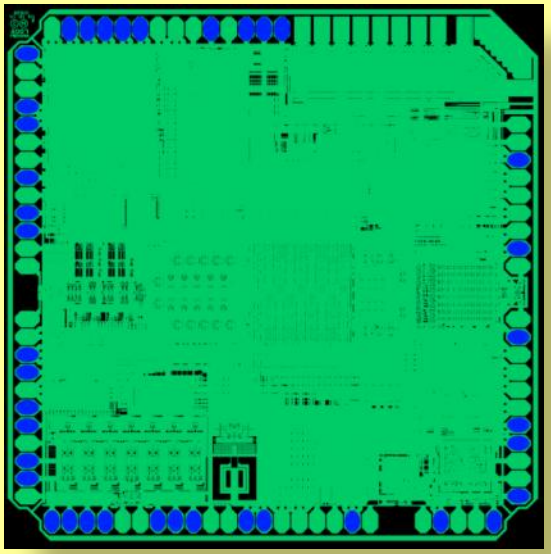
LVS clean ASIC layout



Flattened and removed all non-metal layers



Added pins corresponding to the power plane of interest (ground net in this case)



for simplicity same color is assigned to all layers

ACCURATE IR DROP SIMULATION METHODOLOGY
Step #2: Simulation & Data Collection

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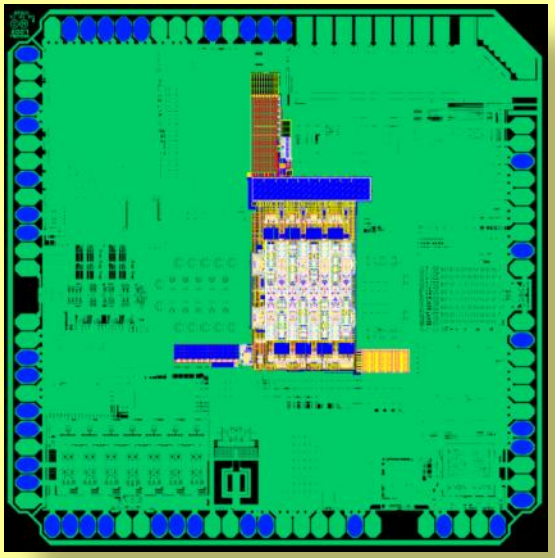
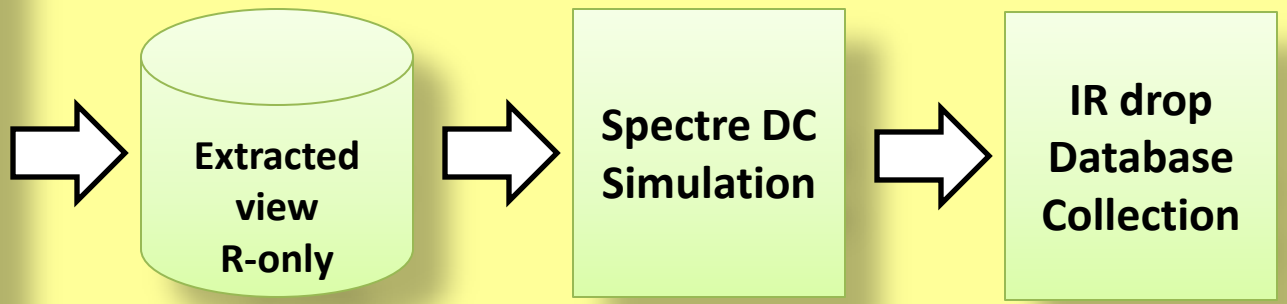
Prepared power plane layout cell is instantiated into block layout. Calibre or Assura R-only extracted view is created and used for Spectre DC simulations. Simulation results are fed to Skill script which builds databases of IR drop by traversing through parasitic resistors instances in the extracted view. Script measures voltage across parasitic resistors terminals and collects coordinates of the corresponding metal fragments. Procedure is repeated for each of the blocks of interest using same power plane layout cell.





ACCURATE IR DROP SIMULATION METHODOLOGY
Step #3: Visualization

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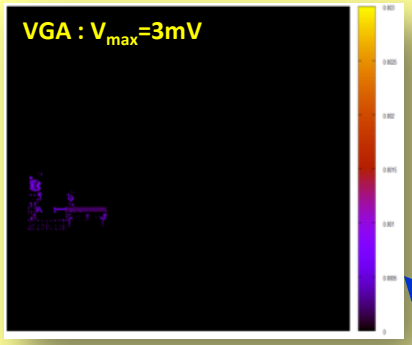
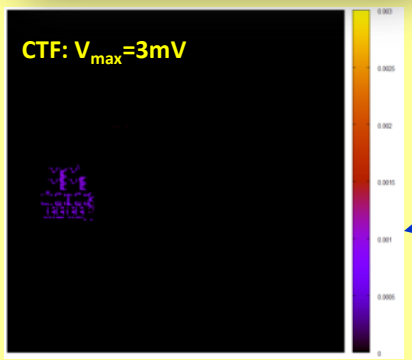
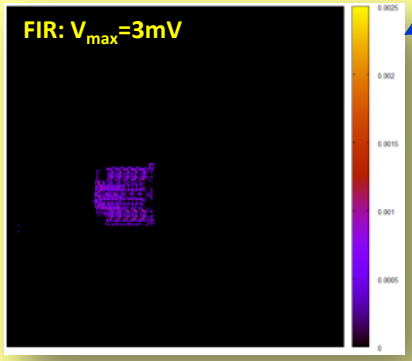
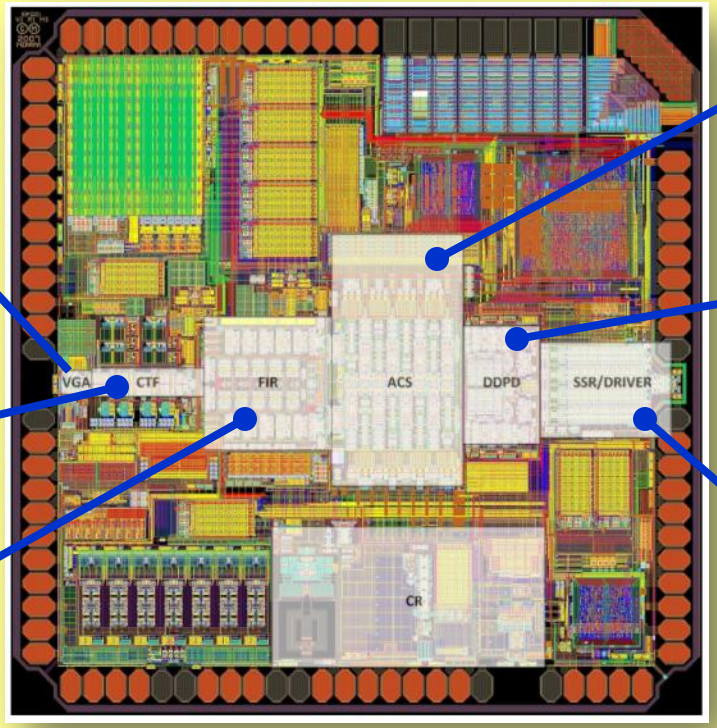
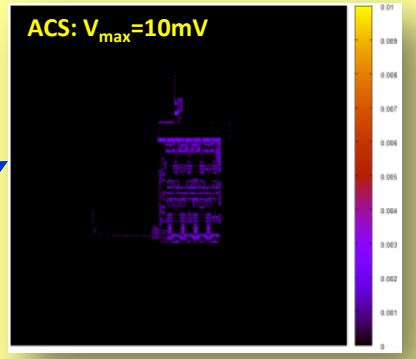
IR drop database content presented using color map

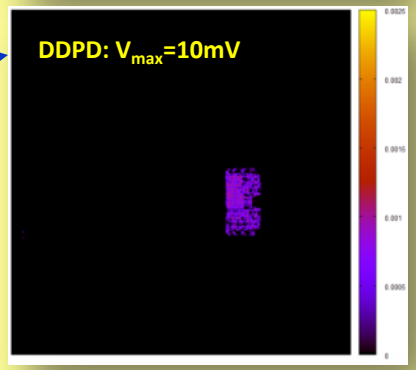


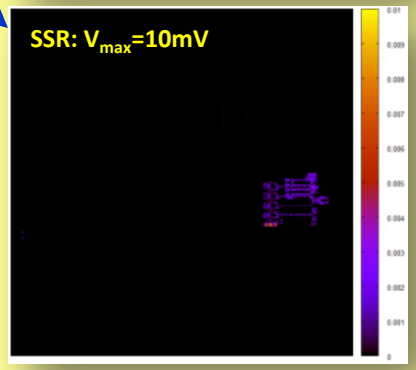






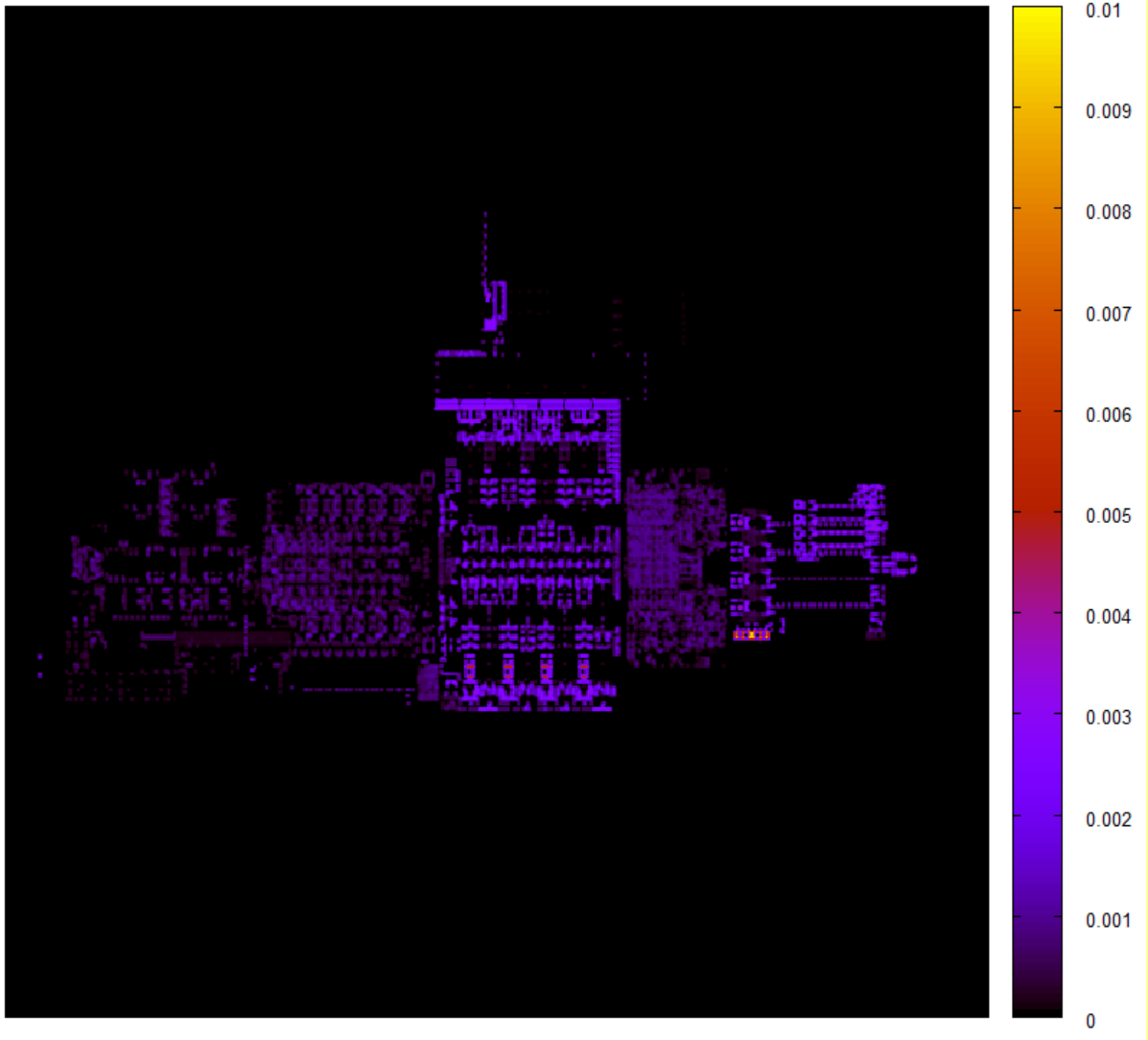






Simulation results can be combined into a chip-scale map of IR drops caused by all current consuming blocks.

ACCURATE IR DROP SIMULATION METHODOLOGY
Step #4: Analysis of IR Drop Severity



- Final IR drop map of ASIC ground plane with 6 top level blocks (~90% of power) taken into account.
- Maximum IR drop across the die is 10mV.

ACCURATE IR DROP SIMULATION METHODOLOGY
Step #5: Visual identification of troubled areas/blocks

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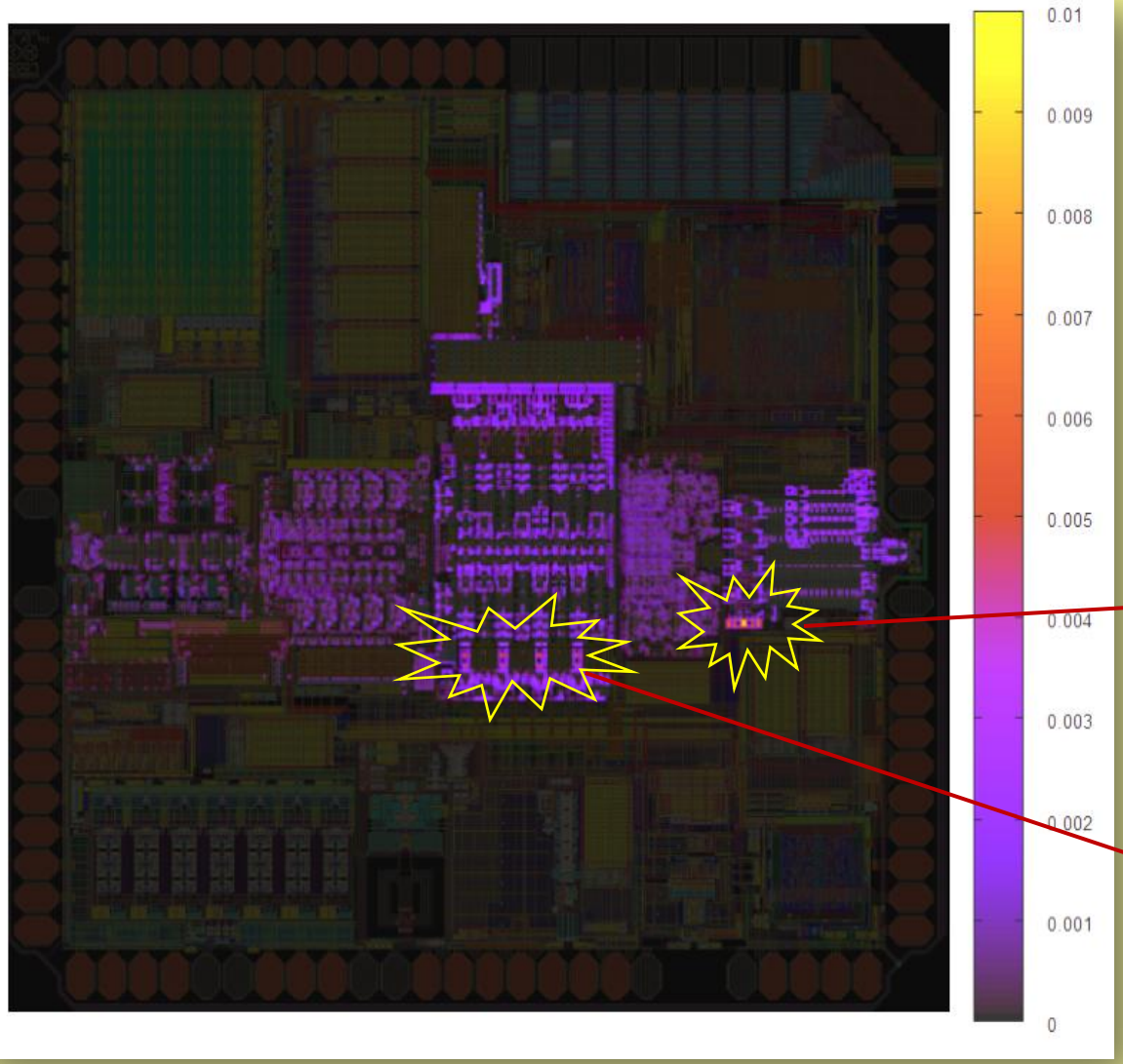
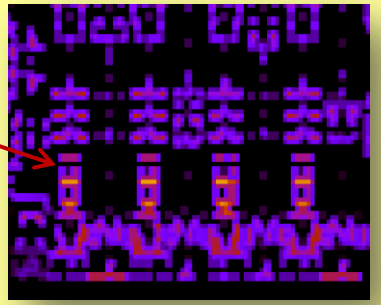


Resulting IR drops are mapped on ASIC layout to pinpoint problematic areas.

Bright yellow spots indicating the largest voltage drops correspond to the potential current density violations and should be reviewed.



Summary

- We presented an accurate grid IR drop simulation methodology.
- Methodology can be plugged into any analog IC design flow for a power grid sign-off.
- Demonstrated simulation result of PRML fiber optics receiver ASIC ground plane shows 10mV voltage drop across the die.
- IR drop visualization allows to locate possible metallization reliability issues.

CONCLUSIONS

Pacific MicroCHIP Corp.

- We presented 2 additional steps for analog intensive ASIC design flow: thermo-electrical simulations and accurate IR drop simulation.
- These methodologies were applied during design of PRML based EDC fiber-optic receiver ASIC and contributed to its 1st pass success.
- Both steps utilize CAD tools commonly used in IC design flow