

A Monolithic One-sample/bit Partial-Response Maximum Likelihood SiGe Receiver for Electronic Dispersion Compensation of 10.7Gb/s Fiber Channels

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Abstract: Combining a 1-sample/bit monolithic PRML receiver with standard MZM modulators and PIN receivers, we experimentally demonstrate error-free transmission (with standard G709 FEC) over a 400-Km uncompensated standard mode fiber link.

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1. Introduction

Maximum-likelihood sequence estimation (MLSE) has been shown to be a powerful technique for electronic compensation of both chromatic and polarization mode dispersion [1-3]. For the first time, to our knowledge, we propose a receiver based dispersion mitigation technique based on the principles of partial-response maximum likelihood equalization (PRML), and experimentally show its superior performance, in terms of achievable reach, over existing EDC solutions employing intensity modulation and direct detection (IM-DD). Its achievable reach (over 400Km of uncompensated standard mode fiber) paves the way for a seamless and instant 10G upgrade of existing 2.5G optical networks, only requiring the placement of terminal equipment on an already deployed 2.5Gb/s line system, thus saving capital and operational expenditures in comparison to an entirely new 10Gb/s capable line system.

2. PRML System

PRML is an equalization technique that has been widely used over the past two decades as a means of mitigating intersymbol interference (ISI) in magnetic [4] and optical storage media. Figure 1, depicts a high-level block diagram of a typical PRML system. Prior to transmission over the channel, the data is first precoded using an appropriate partial-response (PR) coder. This coder, which has a unity coding rate (i.e., adds no overhead), prevents catastrophic error propagation during data recovery at the receiver. Next the precoded data is applied to a transmitter with a given pulse response and transmitted over the channel $H(w)$, which in this case the transmitter is a standard MZM modulator and the channel is standard mode fiber. Likewise, an Electro Absorption (EA) intensity modulator may be used since no phase change information is required for the PRML system. Upon reception and optical-to-electrical conversion (OE), the signal is applied to a matched filter (matched to the combined transmitter, channel and OE response) whose function is to optimize the detection signal-to-noise ratio (SNR). The filtered signal is sampled then applied to a PR filter, typically implemented as finite impulse response (FIR). This is a crucial step and a key differentiator between PRML and standard MLSE equalization. The PR filter function is to shape the frequency response of the received signal into a predetermined partial response of the form $(1-D)(1+D)^n$ (the $(1-D)$ term can be dropped for signals with non-zero DC content), where D is the symbol delay and n the PR order. In essence, PR equalization allows for a predetermined amount of ISI in the channel. In doing so, zero-forcing (inverse filtering) is avoided and noise enhancement is significantly reduced. Next the PR equalized filter is applied to a viterbi detector (MLSE) optimized for the given PR channel. Since the signal at the input of the MLSE is predetermined and known, no channel estimator is required, as is customary in the standard MLSE. This is the second differentiator and key advantage of PRML equalization over standard MLSE. Moreover, owing to its reduced order, compared to an equivalent inverse filter, PR equalization results in a reduced-complexity MLSE implementation resulting in reduced silicon die size and power consumption for the MLSE circuit. Symbol timing for the entire system is provided by a timing recovery block whose task is to recover the clock, with precise frequency and phase, from the received signal. PR post coding, the inverse function of the precoder, is the last step in PRML data recovery. This implementation uses a class-2 partial response, PR2, of the form $(1+D)^2$.

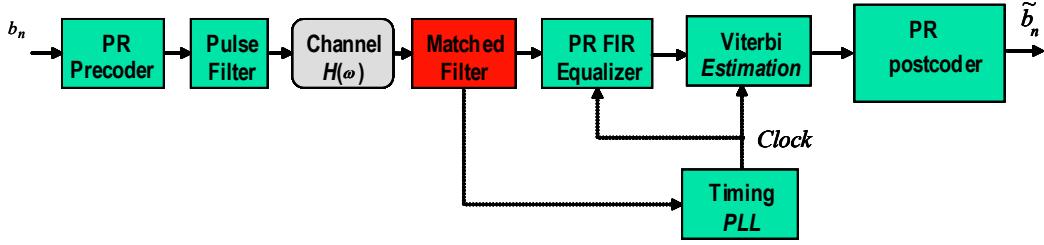


Fig. 1. PRML system block diagram.

3. A Monolithic Discrete-Time Analog PRML Receiver

The ASIC is implemented using an all-analog, 1-sample/bit, track-and-hold based design and does not require the use of high-speed analog-to-digital converters. It is, to our knowledge, the industry's first all-analog implementation of a 10G PRML receiver. Figure 2 depicts a high-level block diagram of our proposed PRML EDC. A 50-ohm differential low-noise variable gain amplifier (VGA) provides necessary gain adjustment for the incoming signal. The gain-adjusted signal is then fed into a tunable constant-group-delay continuous-time filter (CTF) implemented as a 6th order Bessel filter. The filtered signal is next applied to a sampled-analog 5th order FIR filter with adjustable taps. The FIR-CTF are designed to perform class-2 PR equalization. The PR2 equalized signal is then applied to the sampled-analog viterbi detector where branch-metric calculations and survival sequence estimation are performed. The clock recovery (CR) block extracts symbol timing using a minimum-squared error (MSE) decision-directed timing algorithm [5], which provides the sampling clock for the FIR and MLSE blocks. Signal offset is cancelled by an automatic offset control loop that can also be manually adjusted in an open-loop setting. A coarse automatic gain control (AGC) loop using peak detector, PD1, keeps the signal swing constant at the CTF output. The FIR output swing is kept constant by a second AGC loop having a finer step adjustment and employing peak detector, PD2. The recovered data is available at the output of a 50-ohm XFI-compliant, differential output buffer. The ASIC can operate at any rate between 9Gb/s to 11.3Gb/s, is fully programmable and provides a range of test and performance monitoring features available through a compliant serial-parallel interface (SPI). It is fabricated using 0.18 silicon-germanium (SiGe) BiCMOS process and packaged in a 9x9mm ball-grid-array (BGA).

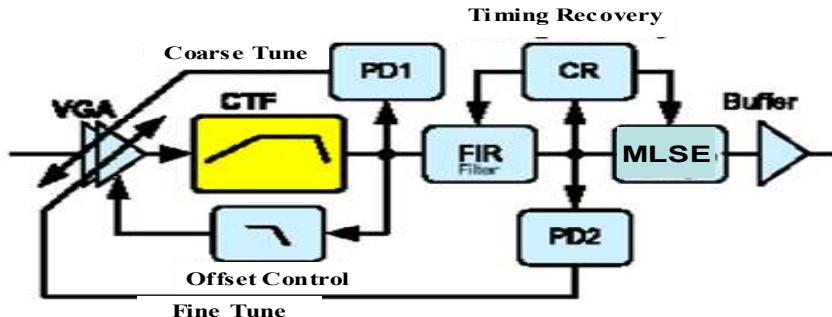


Fig. 2. PRML ASIC block diagram.

4. Experiment Results and Setup

To assess the performance of the PRML receiver, a 2^{31} PRBS NRZ signal modulating a standard MZM device is launched onto an uncompensated 5x80Km-span link (a total of 400-Km of SMF fiber) at a rate of 10.71 Gb/s. The light source is a DWDM 1550nm laser and the link consists of four off-the-shelf erbium-doped fiber amplifiers (EDFA) spaced at 80Km. An optical bandpass filter precedes a standard linear PIN-TIA receiver. Noise loading was performed using an in-line variable optical attenuator. A bit-error rate tester (BERT) was used to detect errors and generate the originating source 10.71Gb/s NRZ signal. Figure 3 depicts the received eye after 320Km of transmission (a), the PR2 equalized eye at the FIR output (b), and the recovered clock and data eye at the ASIC output (c). As can be seen, the received eye is totally shut. PR2 equalization produced the expected $(1+D)^2$, 5-level eye (with residual mis-equalization), which was applied to the 4-state MLSE for NRZ data recovery. The required OSNR (for a BER=5E-04) versus

dispersion curve is shown in figure 4. The back-to-back (B2B) required OSNR is around 16 dB and is about 25 dB at 400Km (i.e., 6800ps/nm). The required OSNR increases at a slope of less than 1.5dB/80-Km-span (or 1.5dB/1360ps/nm) for the first 3 spans. Over the last two spans the slope increases to about 2.5dB/span. The curve is well-behaved and has a mild rate of increase suggesting that further reach can be achieved. The recorded B2B OSNR is higher than has been reported by other similar publications but the realized reach of this receiver exceeds by a good margin those of all reported EDC receivers employing standard NRZ transmission and direct detection (non-coherent, IM-DD) means. It is also worth mentioning that the superior performance of this PRML receiver was achieved using only a 1-sample/bit and a 4-state MLSE.

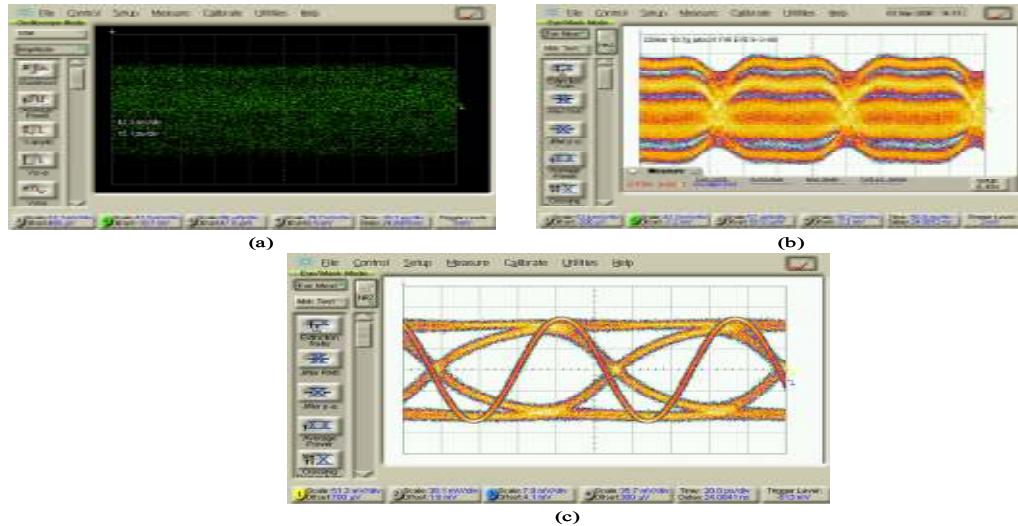


Fig. 3. (a) Eye after transmission over a 320Km uncompensated SMF link, (b) PR Equalized eye, (c) recovered NRZ eye and clock.

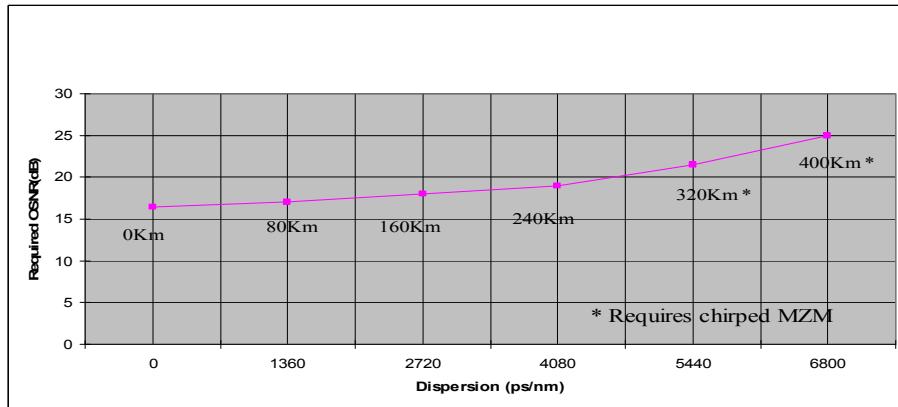


Fig. 4. Required OSNR(0.1nm, BER=5e-4) versus Dispersion.

5. Conclusion

For the first time, a PRML receiver is proposed and experimentally shown to outperform existing MLSE-based receivers. Its novel all-analog implementation allows for a small-form factor monolithic integration and its achievable reach paves the way for a seamless upgrade of 2.5 GB/s optical backhauls to 10Gb/s services.

6. References

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