# Energy Efficient 56 GS/s 8-bit ADC

Keywords: ADC, analog-to-digital conversion, direct RF digitizing, phased arrays

## Technical Summary

Pacific Microchip Corp. is developing an energy efficient 56GS/s 8-bit ADC with ENOB > 6-bit and input bandwidth >20GHz. The chip is fabricated in 28nm CMOS technology node and is assembled on a high performance LTCC BGA chip carrier (12.8mm x 12.8mm). The ADC will be offered as a separate component with the JESD204B standard compliant data interface. In addition, the IP block of the ADC will be offered for integration into ASICs and SoCs.

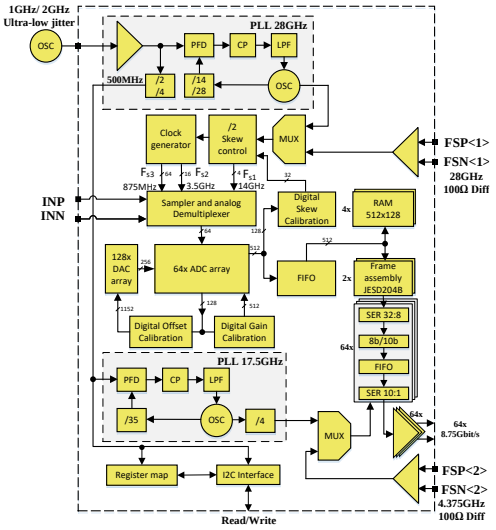



**Figure 1. A block diagram of the ADC chip.**

Figure 2 shows the ADC assembled in a BGA package and an evaluation board mounted on an FPGA development board. The will be supplied to selected customers.

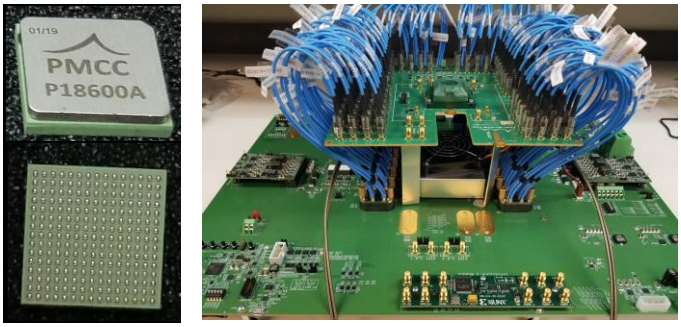



**Figure 2. A BGA package, the evaluation PCB and the test setup.**

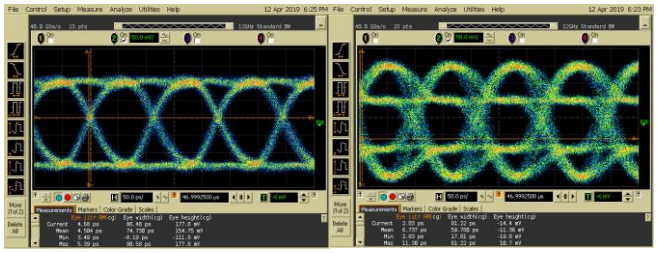


**Figure 3. Tested JESD204B output data eyes. Without pre-emphasis (left) and with pre-emphasis (right).**

## Operational Capabilities

The ADC is expected to offer the best FoM available at ultrafast sampling rates yet providing a reasonable ENOB. The capabilities/features will include:

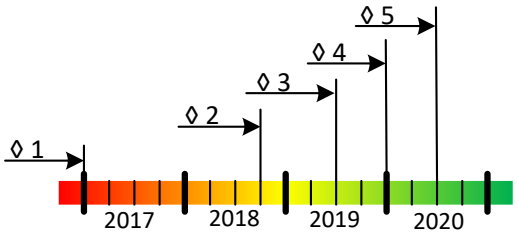
- Sampling rate of 56 GS/s
- Expected ENOB > 6-bit
- Input signal bandwidth > 20GHz
- ADC power consumption 450mW
- FoM < 140 fJ per conversion-step
- JESD204B compatible data output at 64x8.75Gb/s
- Power consumption including JESD interface <2.2W
- On-chip memory of 0.5 Mb for storing digitized data
- I2C interface for control, diagnostics and readout
- 15 x 15 BGA package (12.8mm x 12.8 mm)
- High fidelity, self-calibration

## Development Objectives & Milestones

Pacific Microchip Corp. has demonstrated the feasibility, designed, fabricating the ADC chip which currently is being tested. Further, the chip will be sampled to selected customers. Based on the testing results, the chip will be redesigned, retested, and production will be started.

The project includes the following milestones:

◊ 1. Feasibility is proven based on simulations
◊ 2. Prototype ADC chip is designed and taped out
◊ 3. Prototype chip is fabricated/tested
◊ 4. Final chip is designed and taped out
◊ 5. Final chip is fabricated, tested, and sales are started




Current TRL: 3, Estimated final TRL: 5

## Applications

- Phased antenna array systems
- Software definable radio
- 5G handsets
- Fiber optic transceivers for 100 to 400Gbps
- Spectrum/frequency analyzers
- High sampling rate oscilloscopes
- Satellite communications
- Radio telescopes

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