Spectrometer ASIC

Keywords: Spectrometer ASIC, Earth observation, polyphase filter, FFT, ADC

Technical Summary

This project aims to develop an ASIC for spaceborne and airborne remote sensing instruments. The ASIC is expected to operate with the microwave front ends providing up to 4GHz bandwidth signals. The ASIC includes a VGA, a 6-bit ADC, deserializers, a polyphase filter, an FFT and data analyzing functions. The chip also includes an output data interface, a PLL based frequency synthesizer and a SPI interface for the ASIC's programming (Fig.1). The chip size is 2.5mm x 2.5mm (Fig.2), it is offered in a BGA package (Fig.3) as a separate component and as an IP block for integration into SoCs. An evaluation board (Fig.4) will be supplied to selected customers.

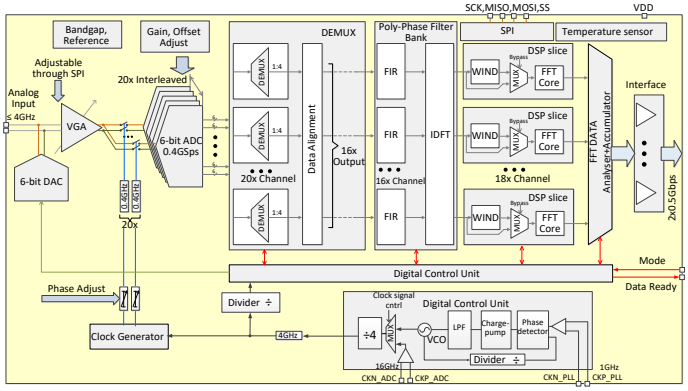


Figure 1. A block diagram of the ASIC.

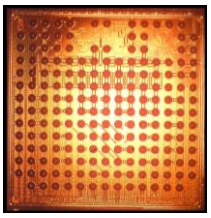


Figure 2. The ASIC's chip photo.

Figure 3. The ASIC in a BGA package.

Figure 4. Evaluation board and test setup with socket.

Operational Capabilities

In the ASIC, the ADC digitizes 0~4GHz RF signal, splits it into 8192 frequency bins, measures the power level in each bin and accumulates the result. Specific capabilities/features include:

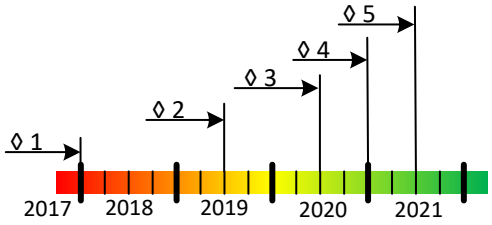
- Input signal bandwidth of 4GHz
- Input signal level 50mV to 400mV pp differential
- Sampling rate up to 8GS/s
- Digitizer ENOB > 4-bit
- Power consumption < 1.8W
- 8192 Frequency bins
- Accumulation time programmable from 5us to 30s
- An integrated 16GHz PLL
- An SPI interface for control, diagnostics and readout
- Temperature range -40°C to 125°C
- 15 x 15 BGA package (12.8mm x 12.8 mm)
- Fabrication technology 28nm CMOS
- Expected TID tolerance > 0.3Mrad

Development Objectives & Milestones

Pacific Microchip Corp. has demonstrated the feasibility, designed and fabricated the ASIC chip which is packaged and is being tested. Further, the part will be sampled to selected customers. Based on the testing results, the chip will be customized for specific application (subject to availability of funds), retested, and its production will be started.

The project includes the following milestones:

◊ 1. Feasibility is proven based on simulations
◊ 2. Prototype ASIC chip is designed and taped out
◊ 3. Prototype chip is fabricated/tested and being sampled
◊ 4. Final/customized chip is designed and taped out
◊ 5. Final chip is fabricated, tested, and sales are started



Current TRL: 3, Estimated final TRL: 5

Applications

- Remote sensing instruments
- Radio astronomy
- Planet and Sun exploration missions
- Synthetic aperture radiometers
- Software-defined radio
- Spectrum analysis

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