A 32 Ch low latency 12b 0.5GS/s ADC

Keywords: Multichannel ADC, analog-to-digital conversion, sensor arrays

Technical Summary

Pacific Microchip Corp. is developing a 32ch. low latency 12-bit 500MS/s ADC. The ADC will be offered as a separate component with the JESD204B standard compliant data interface. In addition, the IP block of the ADC will be offered for integration into ASICs and SoCs.

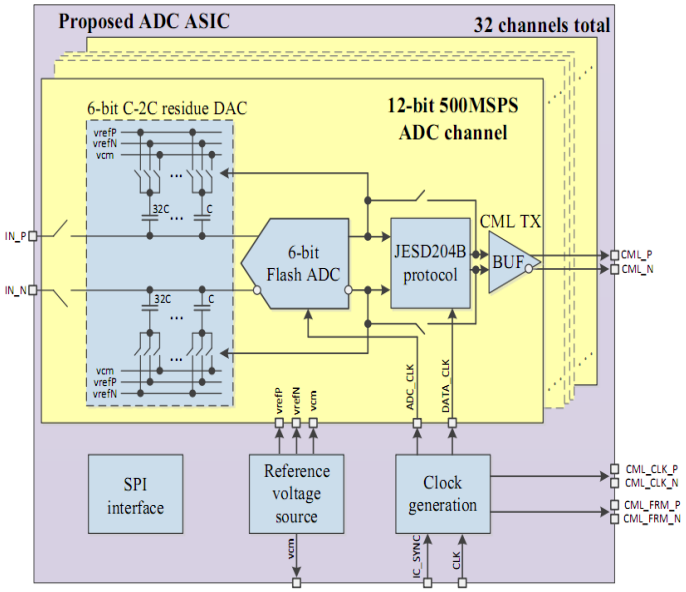


Figure 1. A block diagram of the ADC chip.

The ADC will be assembled in a BGA package (Figure 2) and an evaluation board will be provided to select customers.

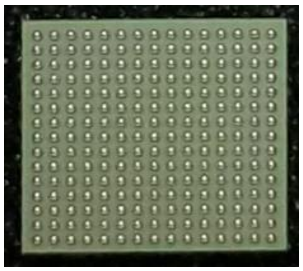


Figure 2. A BGA package.

Operational Capabilities

The 32 independent channel ADC will offer a low latency operation combined with moderate conversion rate and resolution. The ADC features include:

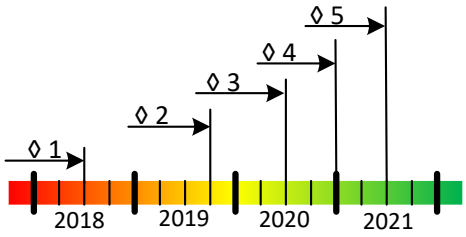
- Low latency (with bypassed JESD interface)
- Sampling rate of 500 MS/s
- ENOB > 10-bit
- 32 channels (independent)
- Input signal bandwidth > 250MHz
- JESD204B output interface with bypassing feature
- Power 40mW/channel (without interface)
- I2C interface for chip control
- Output data rate: 32x8Gb/s
- 28nm CMOS technology
- Estimated die size 10.7mm^2

Development Objectives & Milestones

Pacific Microchip Corp. has demonstrated the ADC's feasibility and is currently in the chip design phase. Further, the chip will be fabricated, packaged, tested and sampled to selected customers. Based on the testing results, the chip will be redesigned, retested, and production will be started.

The project includes the following milestones:

◊ 1. Feasibility is proven based on simulations
◊ 2. Prototype ADC chip is designed and taped out
◊ 3. Prototype chip is fabricated/tested
◊ 4. Final chip is designed and taped out
◊ 5. Final chip is fabricated, tested, and sales are started



Current TRL: 3, Estimated final TRL: 5

Applications

- Sensor arrays
- Test and measurement instrumentation
- MIMO systems
- Radio telescopes
- Synthetic aperture radars and radiometers

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