

# A 6<sup>th</sup> Order 1.6 to 3.2GHz Tunable Low-Pass Linear Phase $g_m$ -C Filter for Fiber Optic Adaptive EDC Receivers

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**Abstract** — A 6th order low-pass 1.6 to 3.2GHz  $g_m$ -C filter for fiber optic adaptive EDC receivers cascades three Bi-Quads permitting reduction of group delay variation down to 10ps. Cut-off frequency is tuned by switching CMOS varactors polarity. THD is below -40dB at 0.9V<sub>pp-diff</sub> output. CTF is implemented in a 0.18 $\mu$ m SiGe process, it occupies 0.17mm<sup>2</sup> and consumes 0.3W from 3.3V supply.

**Index Terms** — Continuous time filters, Tunable filters, High-speed integrated circuits, Optical fiber dispersion

## I. INTRODUCTION

A Continuous Time Filter (CTF) is a critical block in many wire-line, wireless and recently fiber optic systems [1-3]. An analog implementation of Electrical Dispersion Compensation (EDC) in Adaptive Fiber Optic receivers requires a low pass 4-6 order 1.8 to 2.5GHz bandwidth range CTF featuring linear phase (Fig. 1).

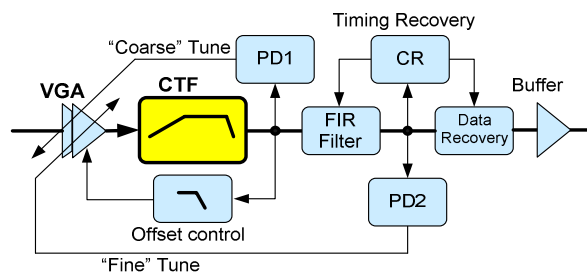


Fig. 1. Block diagram of an analog EDC.

Higher order GHz range filters are currently limited to LC based implementation [4, 5].  $g_m$ -C, also known as OTA-C - is one of the most popular active filter techniques offering the tuning ability and occupying small on-chip area. However, this technique is normally used in the MHz range [6, 7]. We are presenting a small form factor, the  $g_m$ -C based CTF with tunable from 1.6 to 3.2GHz cut-off frequency, a linear phase response and a wide dynamic range.

## II. ARCHITECTURE

The proposed 6<sup>th</sup> order CTF cascades three biquads (Fig. 2). Biquads are implemented as fully differential circuits in order to increase PSRR/CMRR. The low pass frequency response with the linear phase is achieved by setting  $g_m$  of OTA1 equal to  $g_m$  of OTA3 and 3.1 times larger than  $g_m$  of OTA2. OTA3 response is equivalent to resistance equal to  $1/g_m$ . Despite the possibility of power saving, the replacement of OTA3 by a resistor would lead to the increase in CTF parameter variation over process corners.

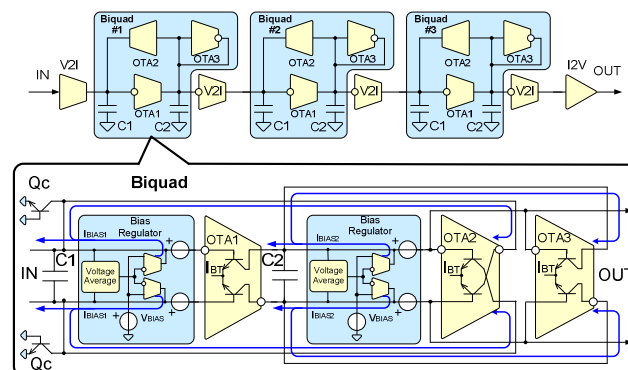


Fig. 2. Block diagram of 6th Order CTF consisting of 3 biquads and the implementation of a differential biquad.

When the cut-off frequency is approached, group delay of a single biquad rolls-off steeper compared to the  $S_{21}$ . Cascading of three biquads reduces the CTF's cut-off frequency  $\sqrt{3}$  times; however, it significantly improves the group delay variation approaching CTF's cut-off frequency. 3.2GHz CTF cut-off frequency requires the biquad's cut-off frequency to be at about 5.5GHz. Inter-stage voltage-to-current (V2I) converters have set their  $g_m$  same as  $g_m$  of OTA2 in order for the biquad to have 0dB

DC gain. This ensures the biquads are operating at the same signal level to enable simpler cascading.  $C_1$  connection node is loaded by one OTA input while  $C_2$  is loaded by three OTA inputs causing the capacitance ratio (ideally 1:1) variation over process corners and temperature. Offset circuits (implemented as emitter followers) provide higher voltage for OTA transistor collectors and help isolating OTA's parasitic loading. Residual loading mismatch is compensated by a circuit represented by  $Q_c$ . OTA bias currents  $I_{BIAS1}$  and  $I_{BIAS2}$  are generated by a circuit that sets the average output voltage at  $V_{BIAS}$ . CTF buffers are designed in such a way as to have their cut-off frequencies exceeding those of biquads in order to minimize the impact on the CTF's performance. The CTF input V2I converter is based on the Cherry-Hooper amplifier (Fig. 3) featuring linearity as well as high speed.

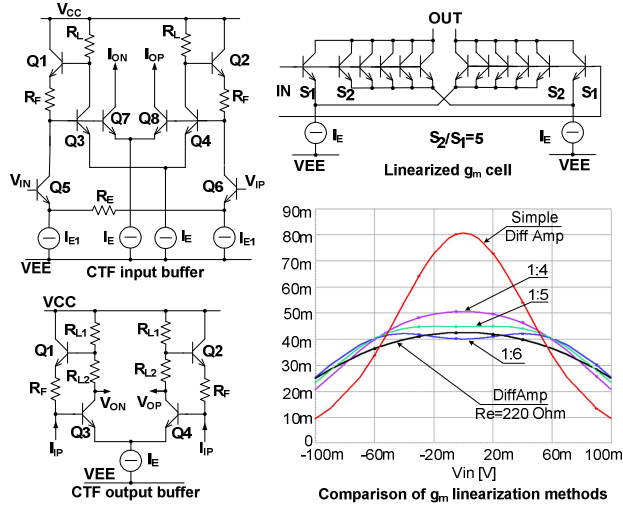


Fig. 3. CTF input and output buffers, a linearized  $g_m$  cell and the comparison of  $g_m$  linearization methods.

Output current is delivered by the diff-pair ( $Q_7$ ,  $Q_8$ ), which replicates  $Q_3$ ,  $Q_4$  as well as V2I converters used between biquads. The CTF output I2V buffer is based on the same Cherry-Hooper configuration. Load resistor  $R_L$  is split to pull up the amplifier input bias voltage in order for the last V2I buffer collector's voltage to be the same as the collector voltage of the other V2I buffers.

The requirement of high frequency at reasonable power limits OTA's architecture to the simplest diff-pair and rules out the possibility of the application of CMOS transistors. The increase of SNR requires the CTF's ability to work with as large signals as possible. The increase of signal levels causes  $g_m$  degradation resulting in compression as well as changing of CTF bandwidth and

group delay. There are several methods that require resistors for the purpose of increasing the dynamic range of a diff-pair. It leads, however, to  $g_m$  varying over process corners resulting from resistance variation. A cross connected rationed as 1:5 diff-pair in our application is found to produce the best linearity (Fig. 3).

Both  $C$  and  $g_m$  are applied in the CTF for the tuning of cut-off frequency  $\omega_c = g_m/C$ . A 3 bit plus "sign" binary coded DAC is programming  $g_m$  (Fig. 4). The current for OTAs is derived as  $5 \cdot (V_{PTAT}/R_{EXT}) - 2 \cdot (V_{PTAT}/R_{INT})$ , where  $R_{EXT}$  and  $R_{INT}$  are respectively external and internal resistors. PTAT reference compensates temperature dependency at the same time  $R_{EXT}$  makes  $g_m$  insensitive to on-chip resistance. The remaining secondary effect of on-chip resistance on the cut-off frequency is compensated by subtracting the part of the current set by  $R_{INT}$ . The resulting current in OTAs is slightly increasing when the internal resistance increases. We limit the current variation by the DAC to a relatively small  $\pm 25\%$  range since  $g_m$  tuning also results in the change of linearity, biasing points and dynamics of OTAs. For this reason, capacitance programming is the preferred method for the tuning of the cut-off frequency. MIM or CMOS capacitors connected in series with CMOS switches is a commonly used method. The combination of the capacitance with the resistance of the switch in ON and OFF states deteriorates a capacitor's  $Q$  and produces unwanted time constants. We are proposing to use CMOS varactors instead of switched capacitors. The back side of the varactor is switched between 1.25V and -1.25V bias with respect to the gate. It changes the capacitance by about 3 times according to Fig. 4 (based on actual data provided by the vendor for  $\pm 3\sigma$  process corners). Most importantly, the back side connection point of the varactors is a virtual ground in a differential circuit. The parasitics introduced to this point by the switches have negligible effect on the CTF's performance. The biasing points are set on the flat portions of  $C(V)$  diagram in order to minimize the capacitance modulation by the signal. Varactor backside can be switched between  $V_{CC}$  and  $2 \cdot V_{BIAS}$  while the gate remains at  $V_{BIAS}$  (Fig. 4). Varactors are scaled as 1:2:4:8 and are combined into a 4 bit DAC (Fig. 4). The implementation of the dual cut-off frequency control allows the use of  $g_m$  tuning (considering its impact on other CTF parameters) for fine adjustment only.

### III. IMPLEMENTATION

A  $0.18\mu\text{m}$  SiGe process is used for the CTF implementation. The die size is  $3.2 \times 3.7\text{mm}^2$  (Fig. 5) with the CTF occupying only  $0.17\text{mm}^2$ . The test chip is wire-bonded in a custom solder bumped package. Before being

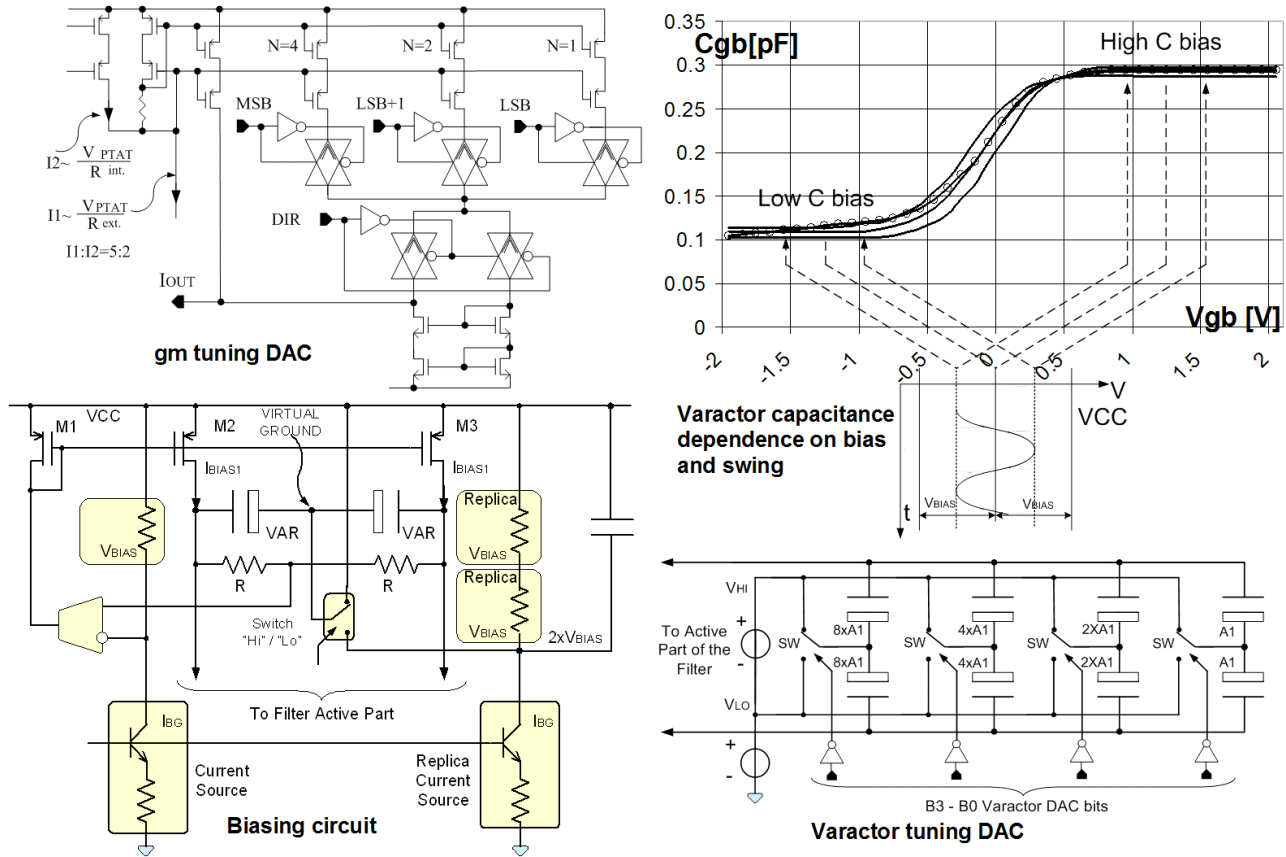


Fig. 4. Schematic of the  $g_m$  tuning DAC, varactor capacitance dependence on bias and swing, the biasing circuit and the varactor tuning DAC.

delivered to the CTF, the signal on the test chip is normalized and has its offset corrected by a VGA. The CTF output signal is buffered and delivered over 1mm

distance to a 50Ohm terminated linear output buffer driving output pads through 50Ohm coplanar transmission lines. SPI is used for the test chip configuration and tuning of CTF bandwidth. The rest of the chip area is used for other functions (beyond the scope of the current presentation) as well as for biasing blocks and power-supply bypassing capacitors.

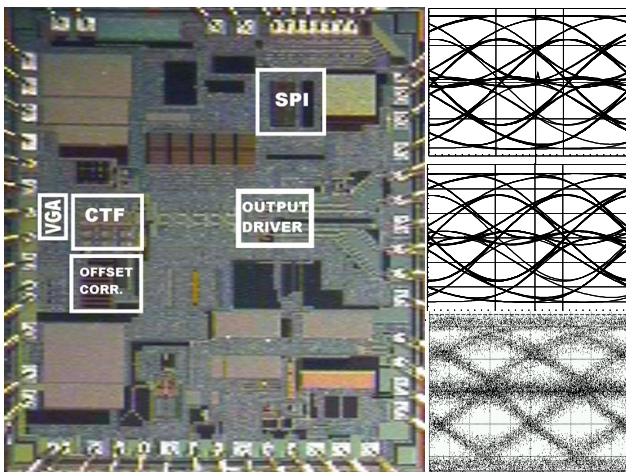


Fig. 5. CTF test chip photo showing the main blocks and CTF output response for 10Gb/s NRZ input data: simulated ideal filter (top), simulated schematics (middle), measured (bottom).

#### IV. CONCLUSION

CTF bandwidth programming range using varactor DAC shows the possibility of covering 1.6 to 3.2GHz range (Fig. 6). The feasibility of covering the frequency range from 1.8GHz to 2.5GHz without using  $g_m$  tuning is also shown. The group delay change is less than 10ps in the frequency range from 0.3GHz up-to cut-off frequency point. The remaining group delay variation with frequency is small enough not to cause any significant visual distortion when comparing ideal, simulated and measured eyes at the CTF output (applied 10Gb/s NRZ data to the input) (Fig. 5). Measured THD at 900mV<sub>pp-diff</sub> output (250mV<sub>pp-diff</sub> input) voltage is below -40dB. Power

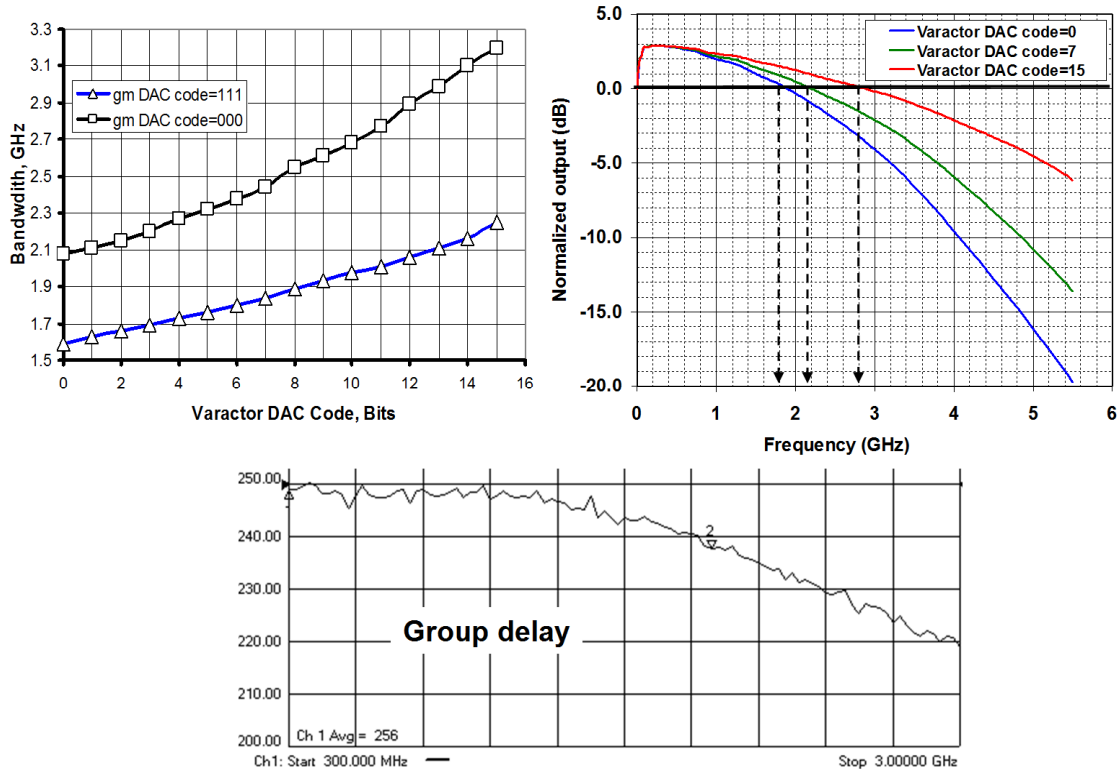


Fig. 6. Measured bandwidth over varactor DAC code, normalized transfer characteristics for 3 values of varactor DAC code and the group delay.

dissipation is 300mW (the output buffer is not included). The CTF transfer characteristics simulated for different process corners (used  $\pm 3\sigma$  process corner combinations) are shown in Fig. 7. Measured data points are overlapped on critical areas of the graph. They closely match the simulations (multiple devices were measured to obtain the data points). The low frequency cut-off point at around 1KHz with 20dB slope is a result of offset control function.

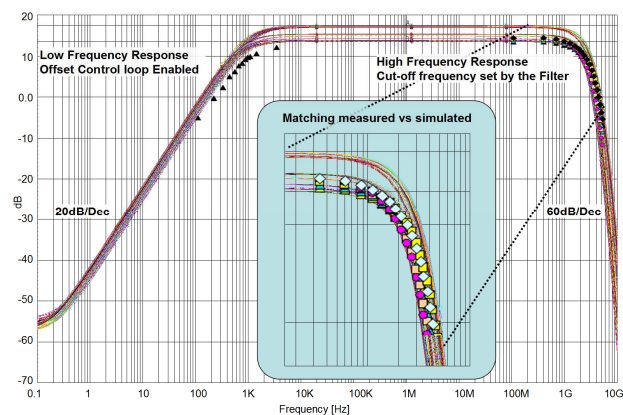


Fig. 7. CTF transfer characteristics – measured vs. simulated.

#### ACKNOWLEDGEMENT

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